

Compal confidential

Liverpool/Sunderland 10AT

NSWAE/NTWAE LA-5332P Schematics Document

Mobile AMD S1G3/
RS880M & RS880MC / SB710

2009-11-24 Rev. 1.0

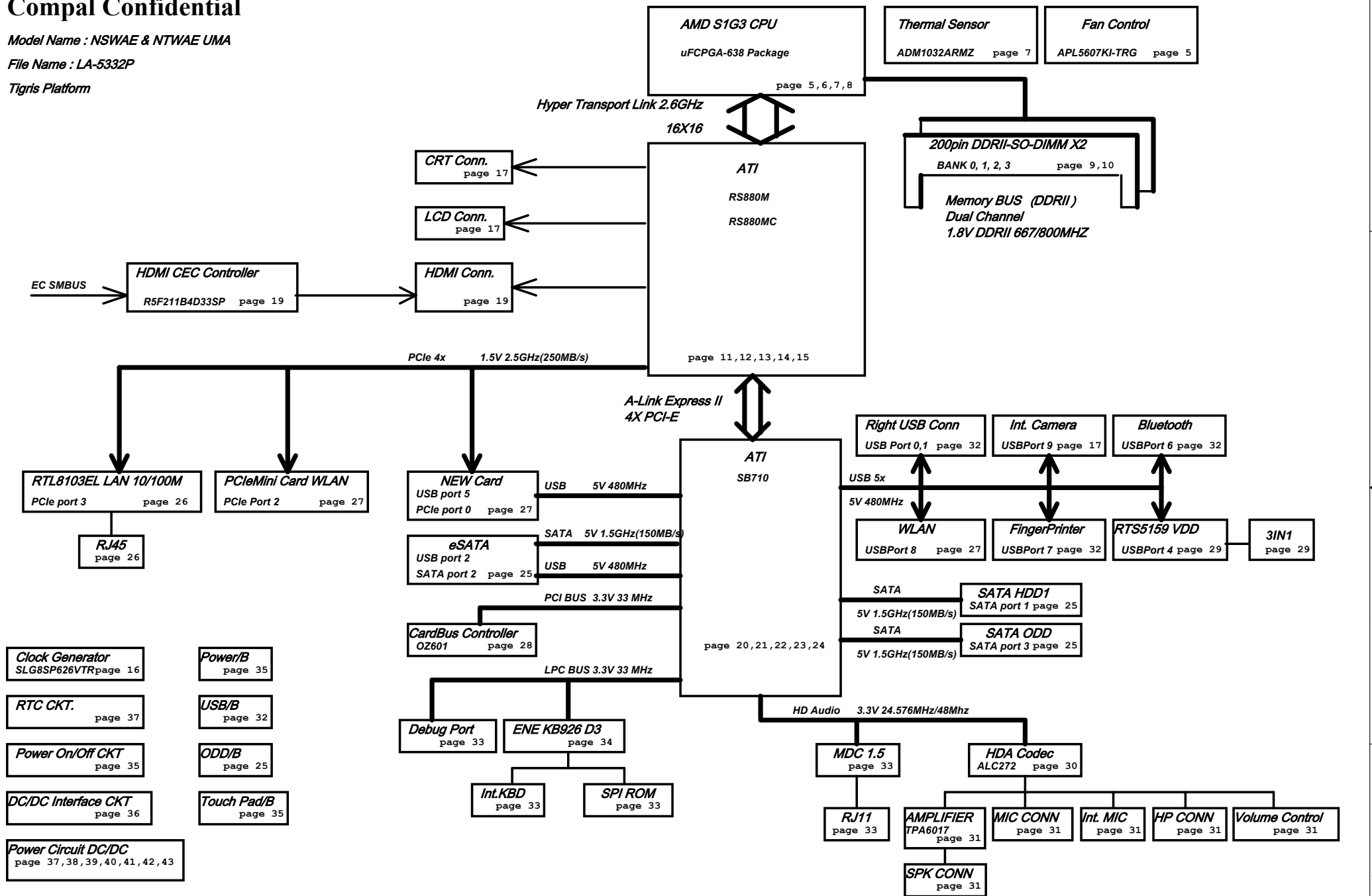
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Model Name : NSWAE & NTWAE UMA

File Name : LA-5332P

Tigris Platform



Clock Generator
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RTC CKT.
page 37

USB/B
page 32

Power On/Off CKT
page 35

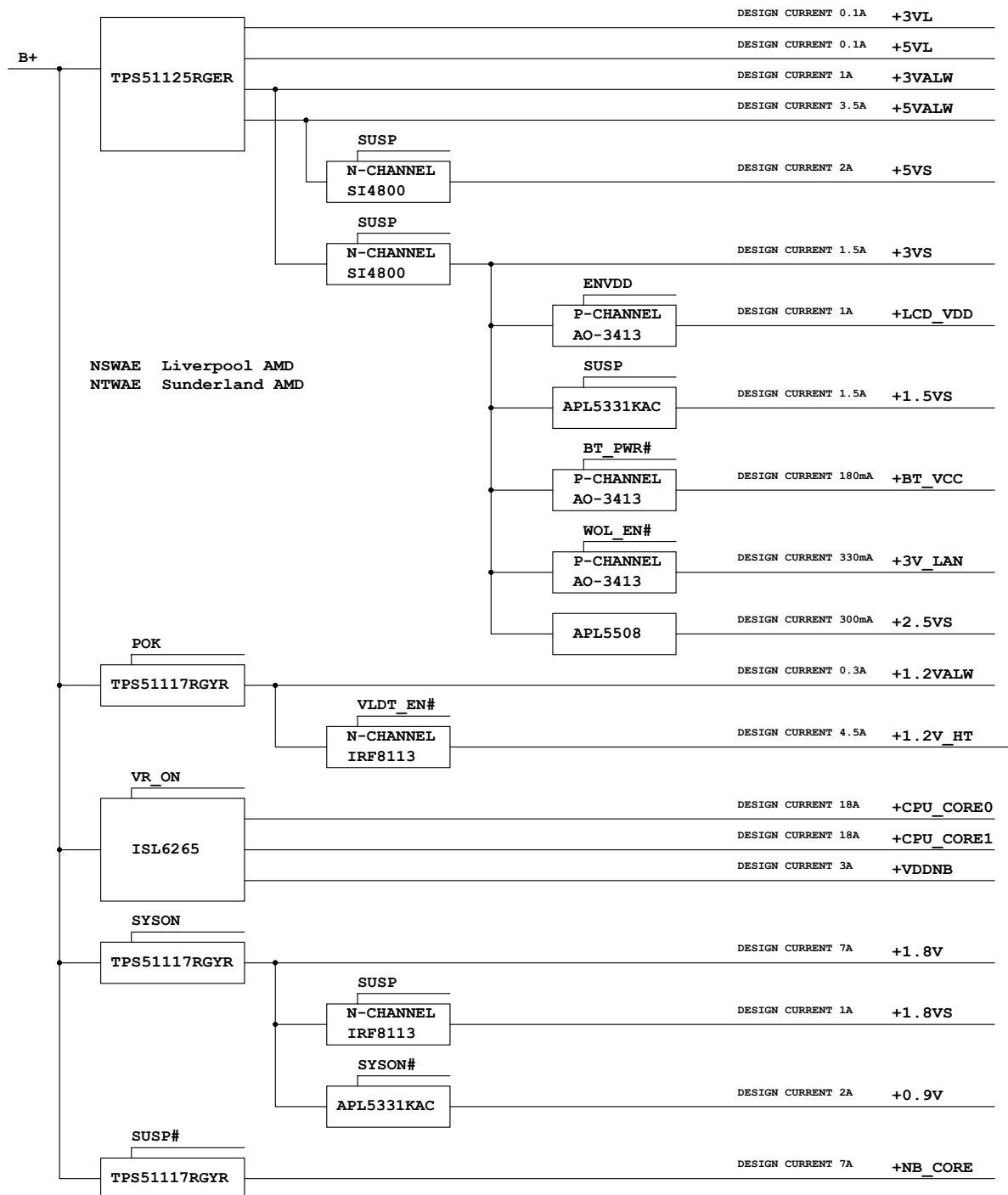
ODD/B
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DC/DC Interface CKT
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Touch Pad/B
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Power Circuit DC/DC
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O : ON
X : OFF

Platform	CPU	NB	VGA	SB	Comment
	S1G3	RS880MC	NA	SB710	
	S1G3	RS880M	NA	SB710	

State \ power plane	+B +3VL +5VL +RTCVCC	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

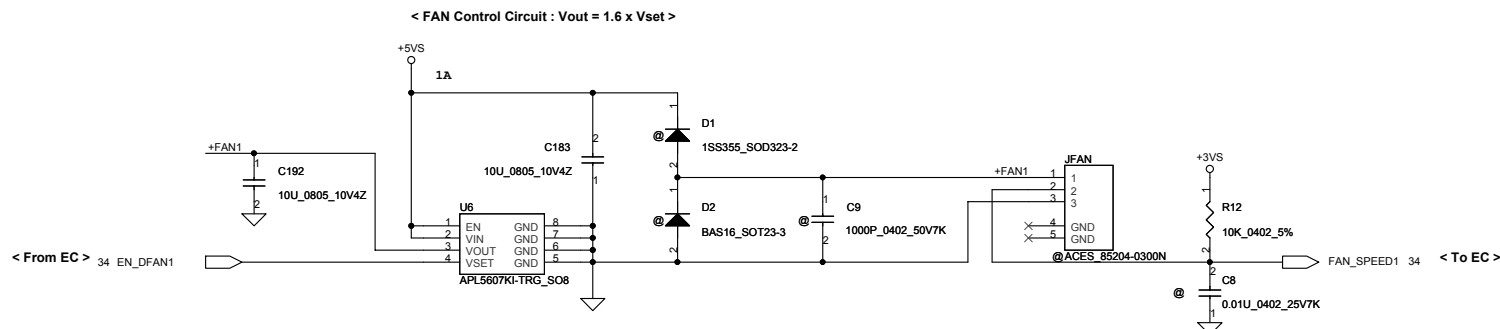
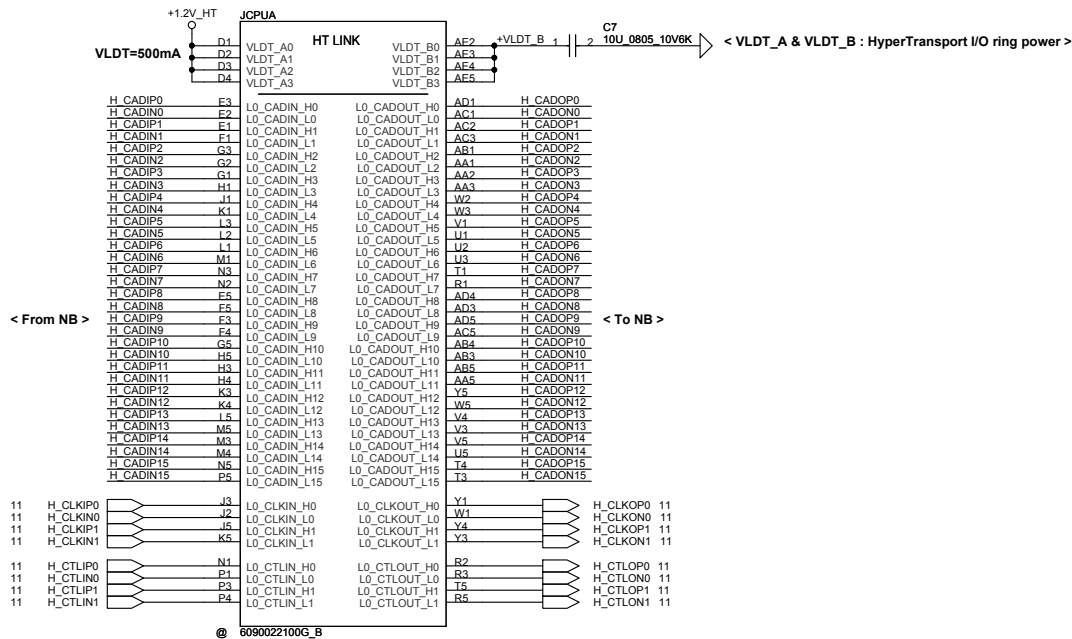
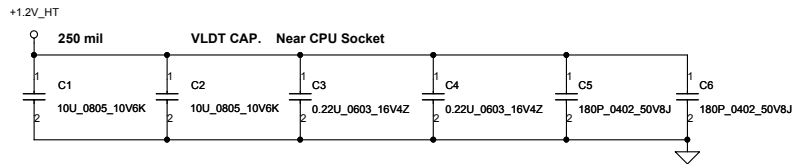
Device	HEX	Address	Device	HEX	Address
Smart Battery	16H	0001 01X b	AD1032-1 CPU	98H	1001 100X b
HDMI-CEC	34H	0011 010X b	AD1032-2 VGA	9AH	1001 101X b
EC KB926D3			EC KB926D3		

Function	Express card / PCMCIA	BLUE TOOTH	RJ11	SSD	SATA ODD		WiFi	HDMI	G- sensor		3 in 1 card reader	FingerPrinter	CAMERA & MIC	
Description	(E / A)	(B)	(R)				(H)	(Y)	(S)		(C)	(F)	(X)	
Explain					16"	17"	Half - size		First	Second	RTS5159		CAMERA	MIC
BTO	EXPCARD@ / PCMCIA@	BT@	MDC@	SSD@	16inch@	17inch@	WLAN@	H@	G@ + G_1st@	G@ + G_2nd@	CARD@	FP@	CAM@	MIC@

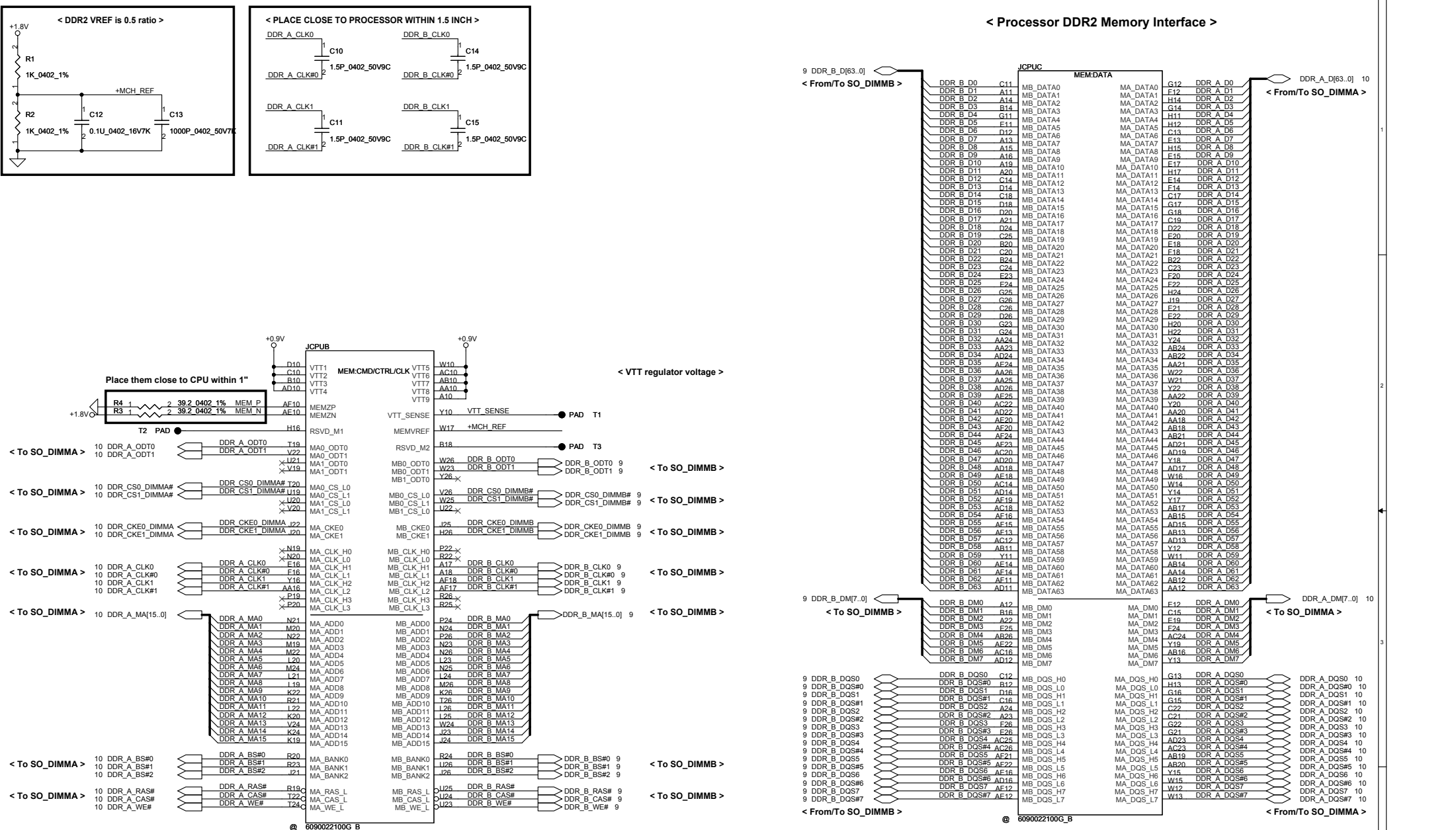
Function	DC-IN		Side port		
Description			(L)		
Explain					
BTO	16inch_45@	17inch_45@	SIDE@	NSIDE@	

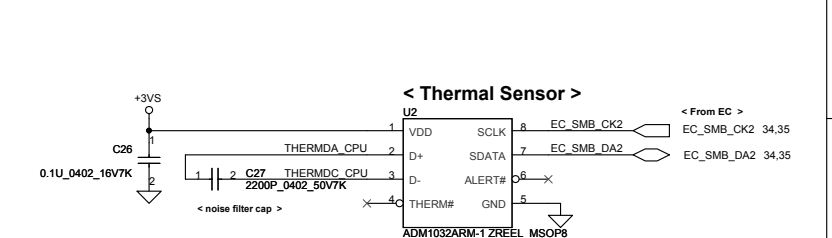
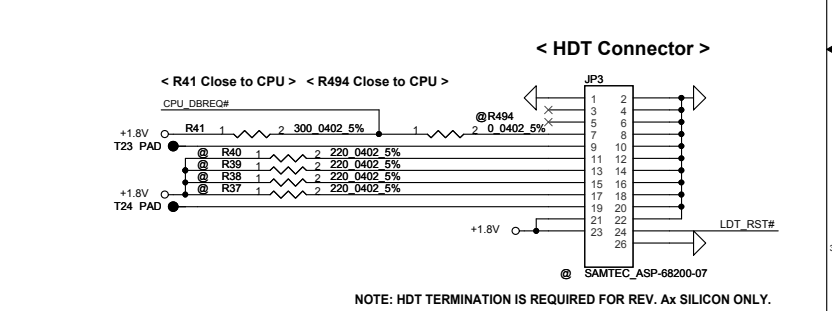
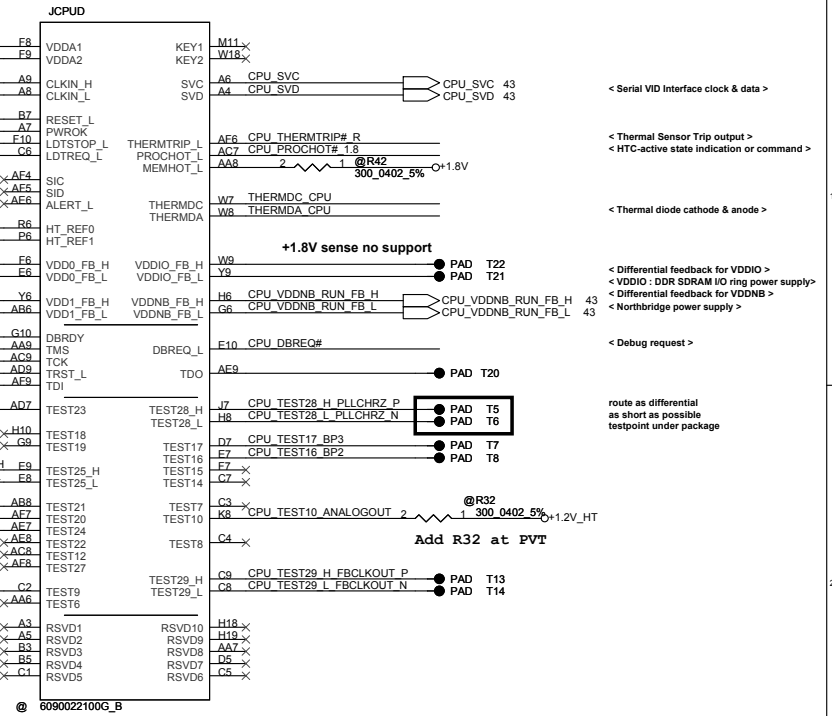
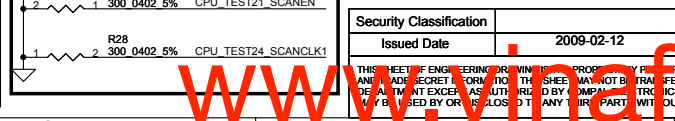
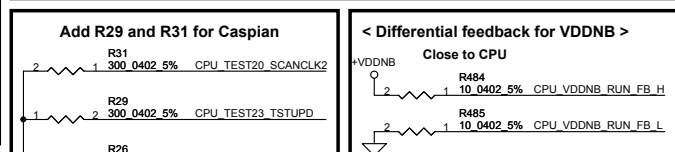
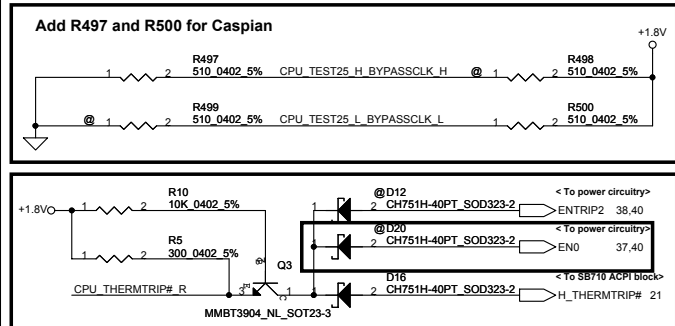
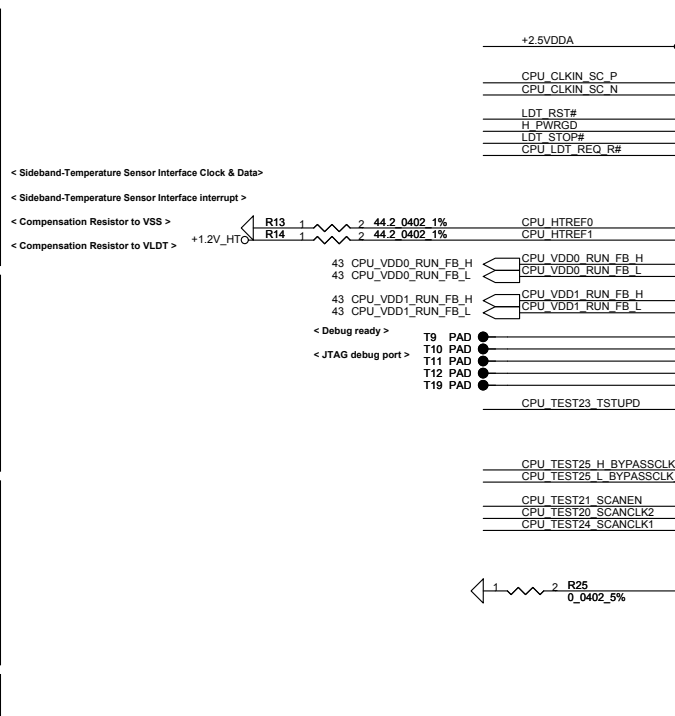
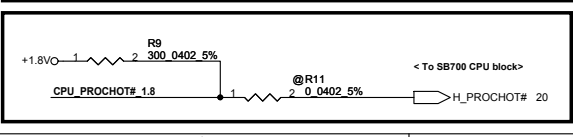
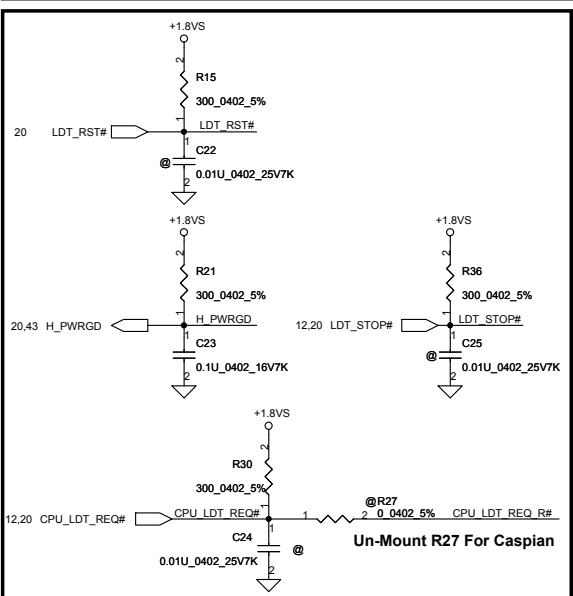
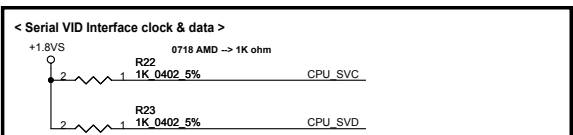
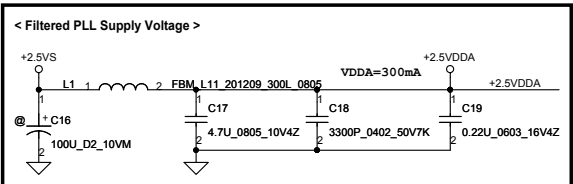
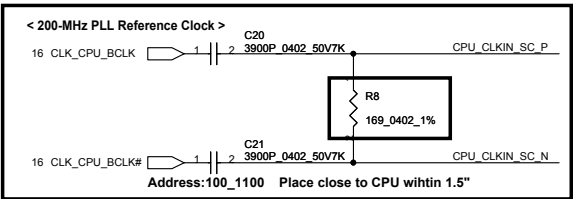
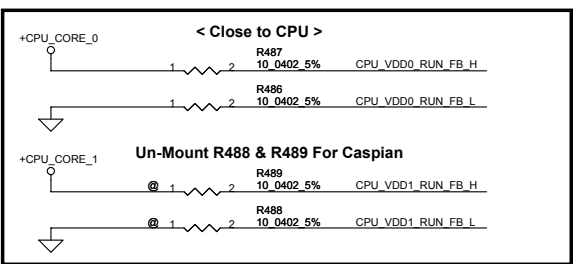
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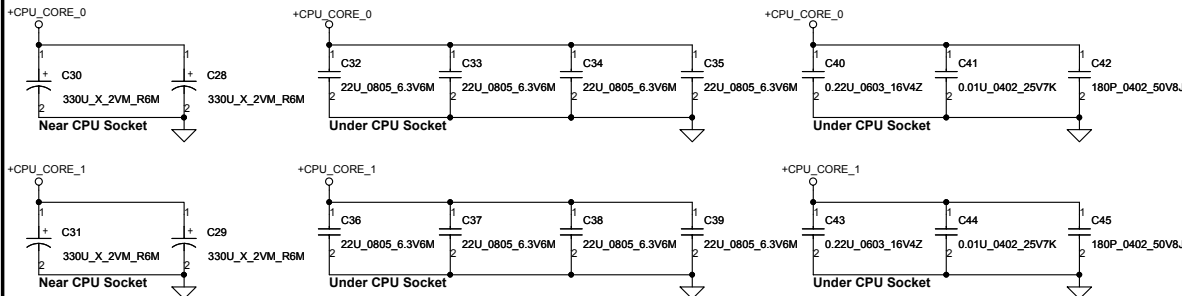
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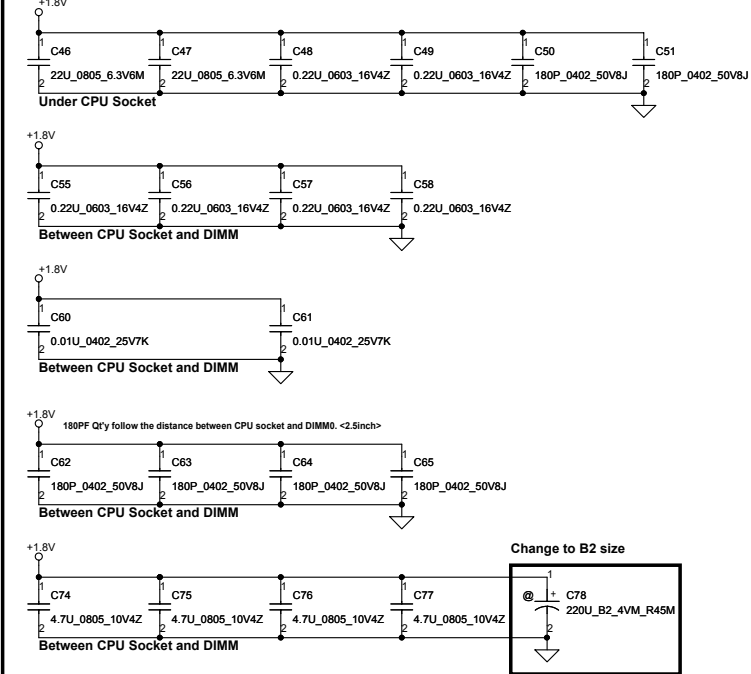


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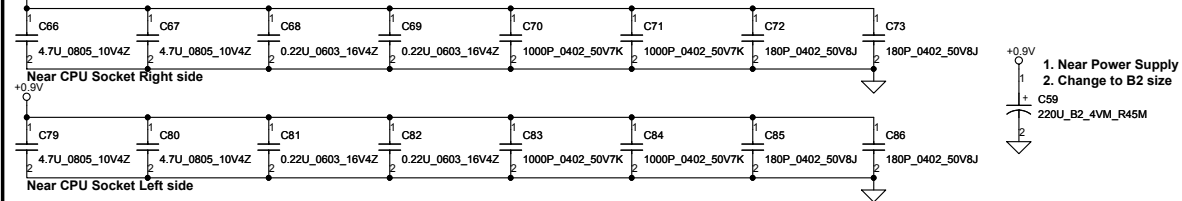
VDD decoupling : +CPU_CORE



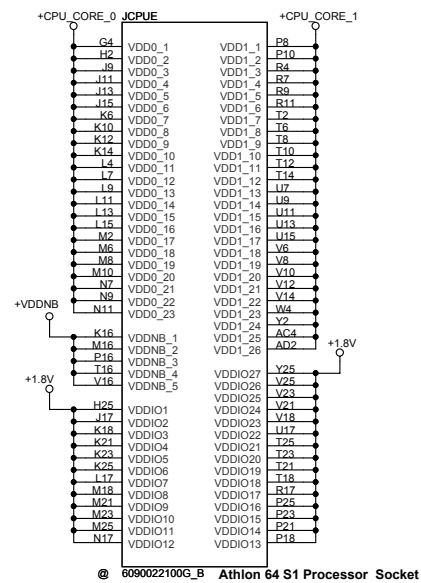
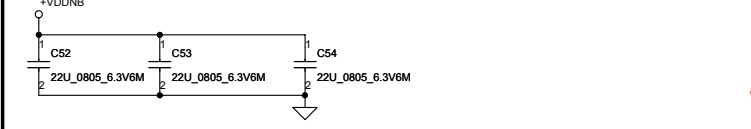
VDDIO decoupling : DDR SDRAM I/O ring power



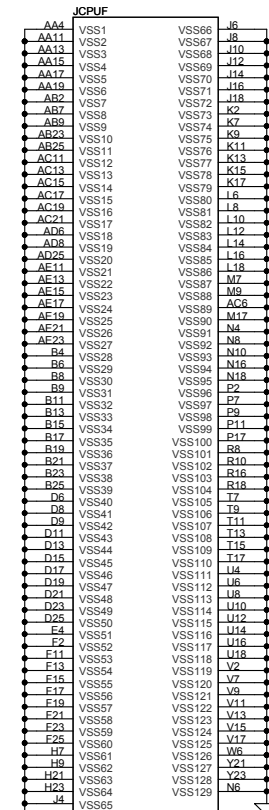
VTT decoupling.



+VDDNB decoupling : Northbridge power

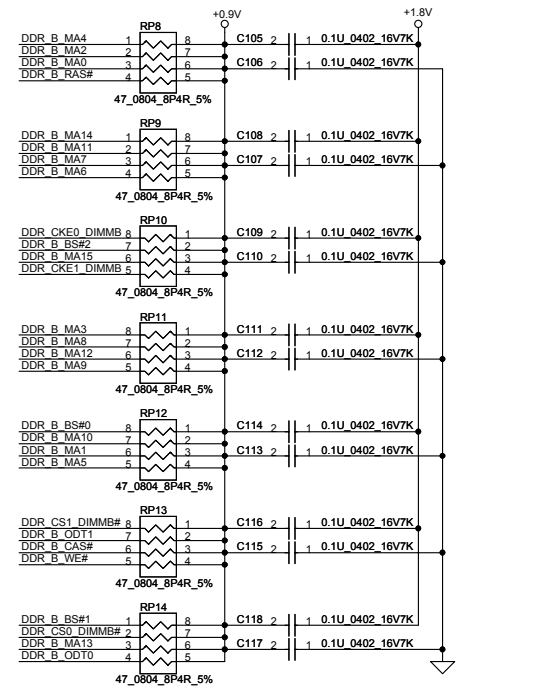
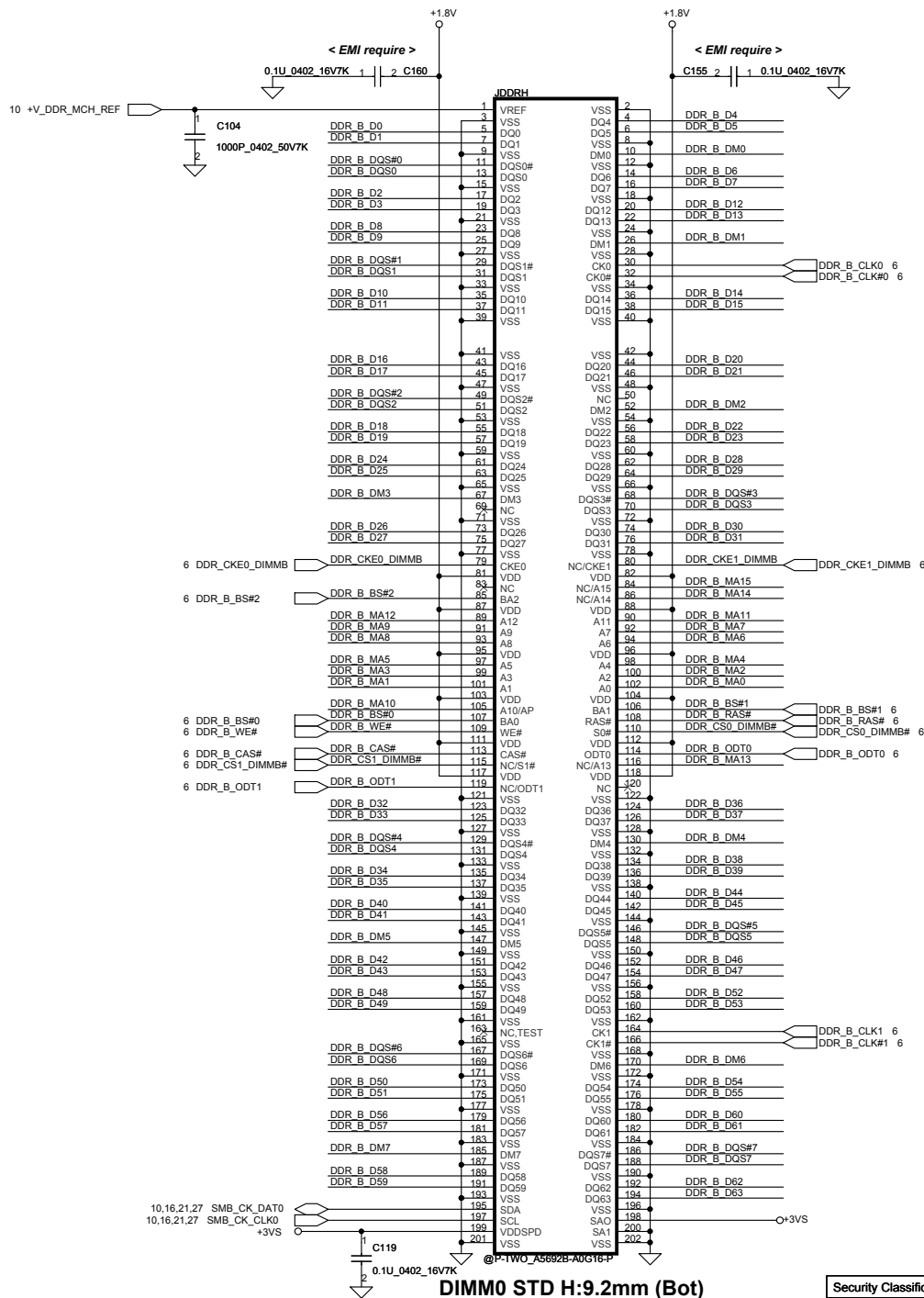


@ 6090022100G_B Athlon 64 S1 Processor Socket



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DDR B D[0..63] 6

DDR B DM[0..7] 6

DDR B DQS[0..7] 6

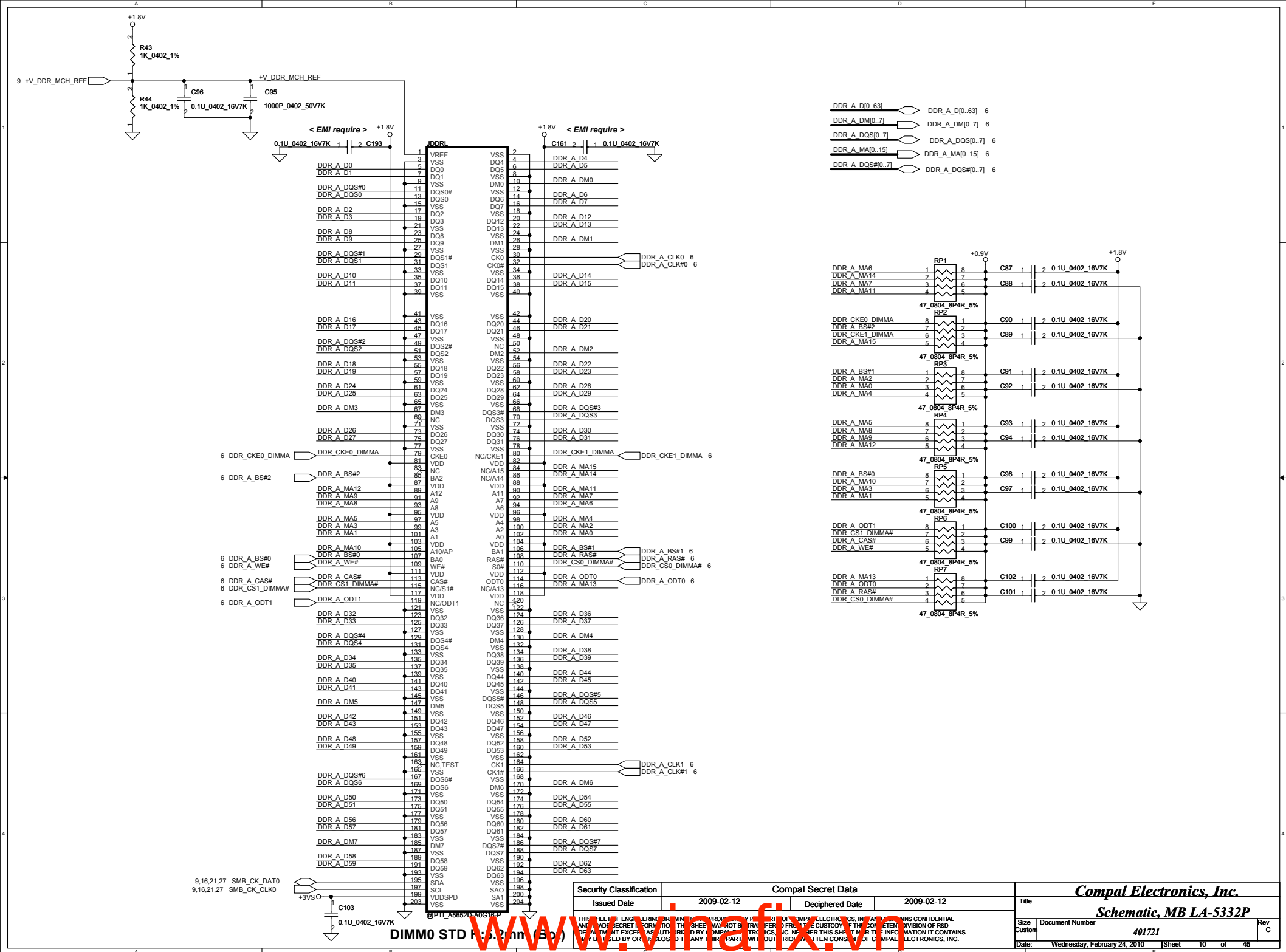
DDR B MA[0..15] 6

DDR B DQS#0..7 6

DIMM0 STD H:9.2mm (Bot)

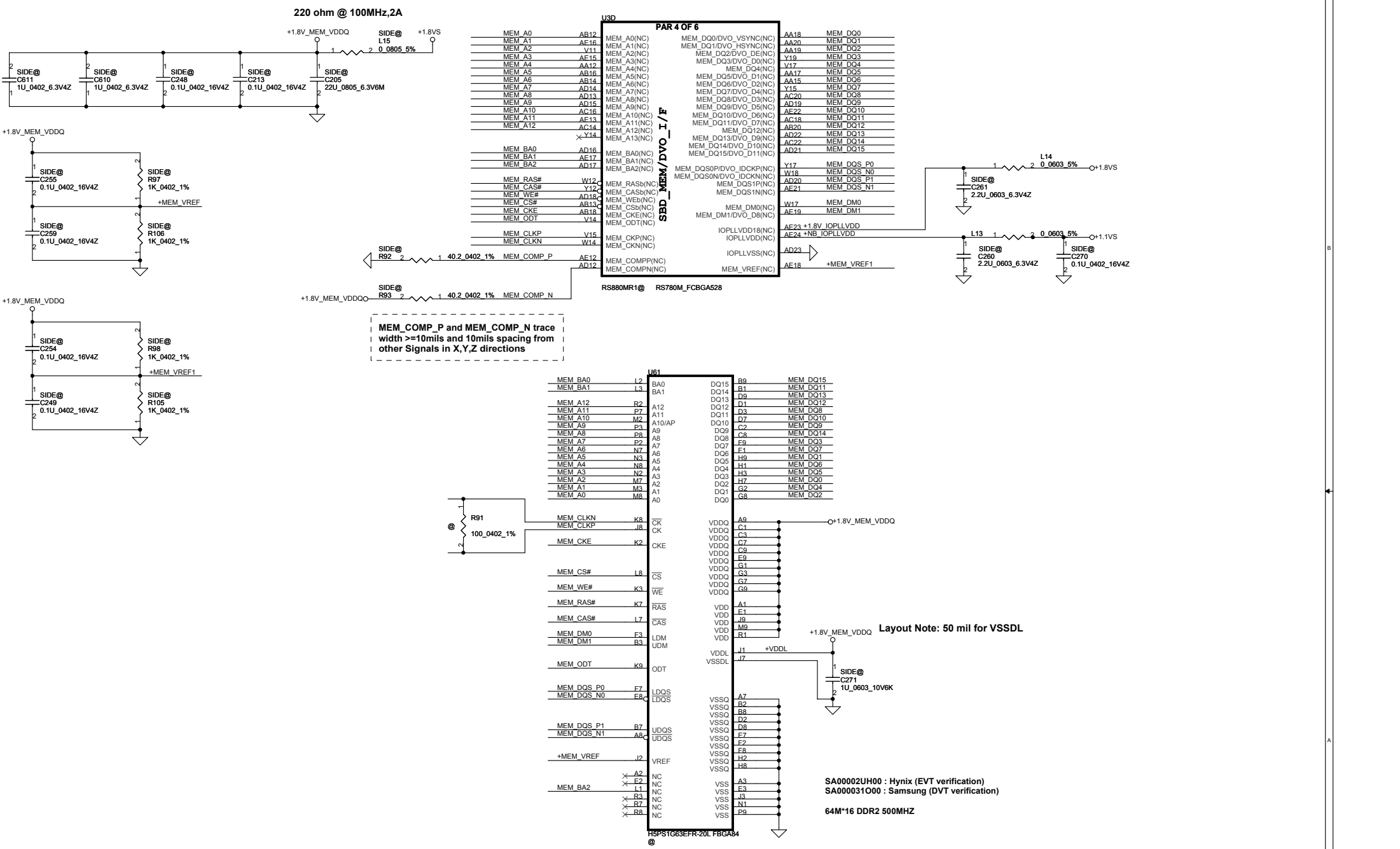
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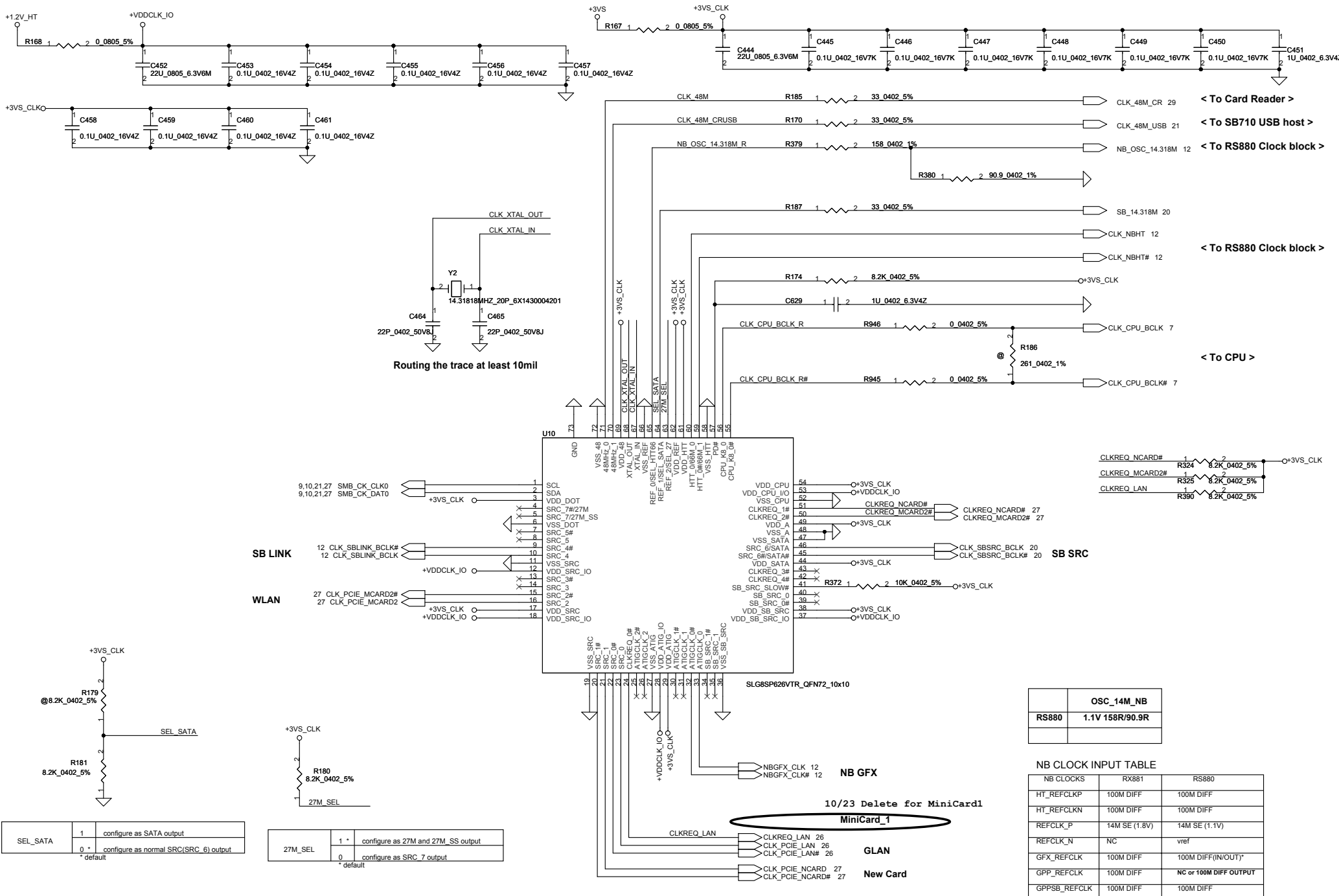




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<p>< RS880 VSYNC mux at CRT_VSYNC pull High to 3K ></p> <p>SI2: Change to 3K pull high</p>	<p>< VSYNC : STRAP_DEBUG_BUS_GPIO_ENABLEb ></p> <p>Enables the Test Debug Bus using GPIO.</p> <p>1 : Enable (RX881, RS880) 0 : Disable (RX881, RS880)</p> <p>PIN: RS880--> VSYNC#</p>
<p>< RS880 use register to control PCI-E configure ></p>	<p>< DFT_GPIO[4:2] : STRAP_PCIE_GPP_CFG[2:0] ></p> <p>These pin straps are used to configure PCI-E GPP mode.</p> <p>000 : 00001 001 : 00010 010 : 01011 011 : 00100 100 : 01010 101 : 01100 111 : 01011</p>
<p>< RS880 SUS_STAT# ></p>	<p>< SUS_SATA# : LOAD_EEPROM_STRAPS ></p> <p>Selects Loading of STRAPS from EPROM</p> <p>1 : Bypass the loading of EEPROM straps and use Hardware Default Values 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected</p> <p>RS880:SUS_STAT#</p>
<p>< RS880 use HSYNC to enable SIDE PORT (internal pull high) ></p>	<p>< HSYNC : STRAP_DEBUG_BUS_PCIE_ENABLEb ></p> <p>RX881: Enables the Test Debug Bus using PCIE bus</p> <p>1 : Disable (Can still be enabled using nbcfg register access) 0 : Enable</p> <p>RS880: Enables Side port memory (RS780 use HSYNC#)</p> <p>1. Disable (RS880) 0 : Enable (RS880)</p>



SEL_SATA	1	configure as SATA output
	0 *	configure as normal SRC(SRC 6) output * default

27M_SEL	1 *	configure as 27M and 27M_SS output
	0	configure as SRC 7 output * default

Use voltage divider resistor R379 & R380 to pull low

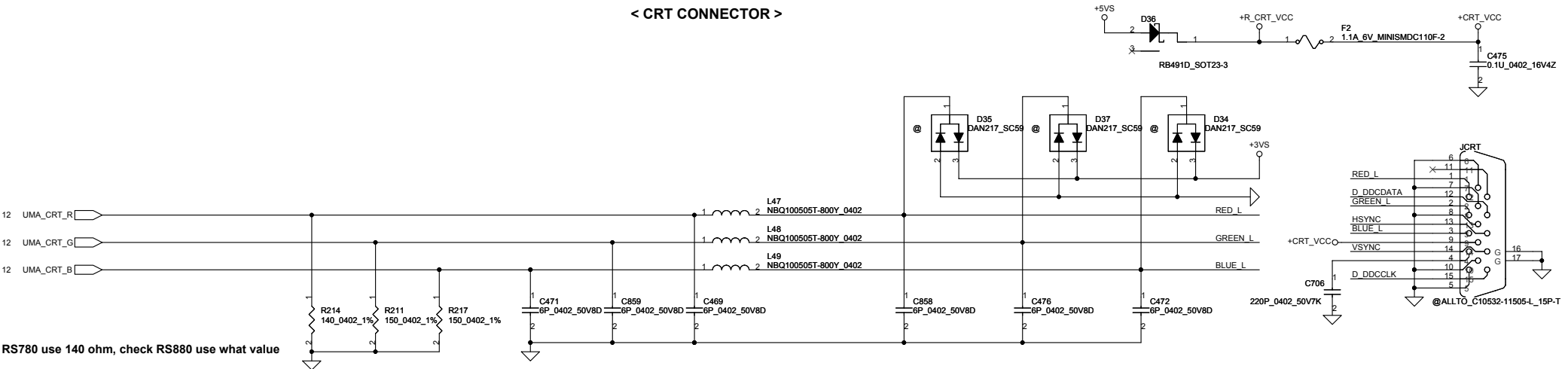
NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output * default

	OSC_14M_NB
RS880	1.1V 158R/90.9R

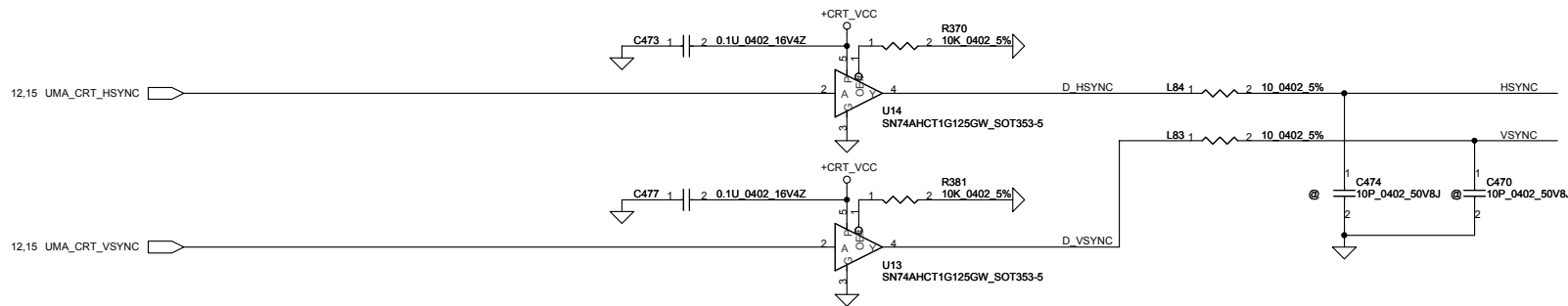
NB CLOCK INPUT TABLE

NB CLOCKS	RX881	RS880
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

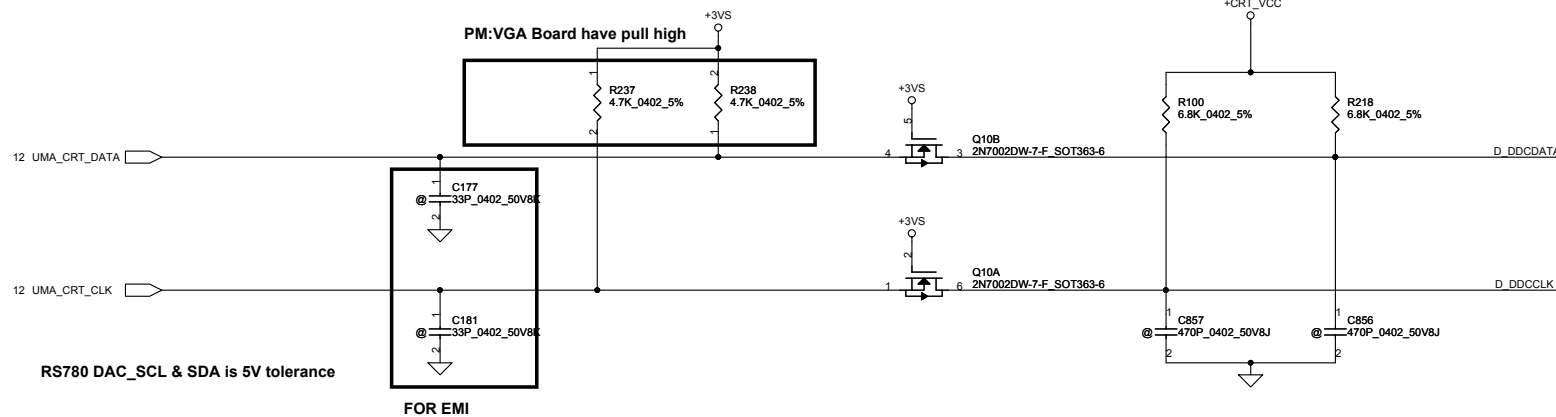
< CRT CONNECTOR >



< SYNC SIGNAL >



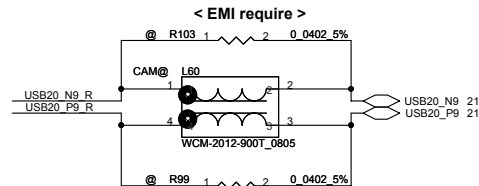
< Display Data Channel >



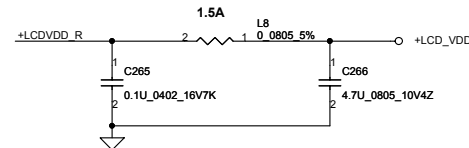
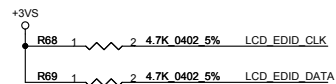
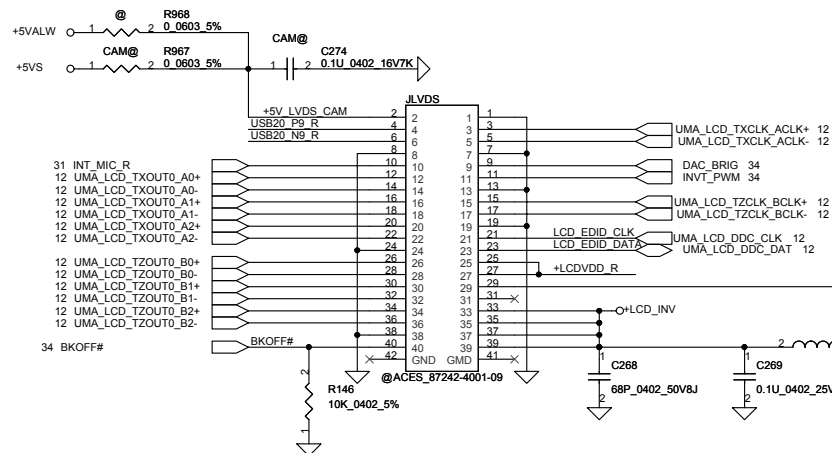
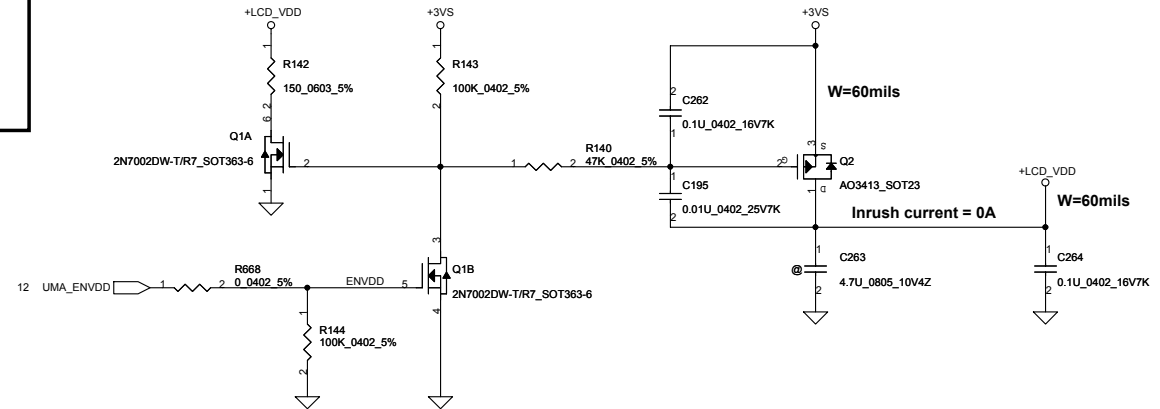
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< Int. Camera, USB port 9 >



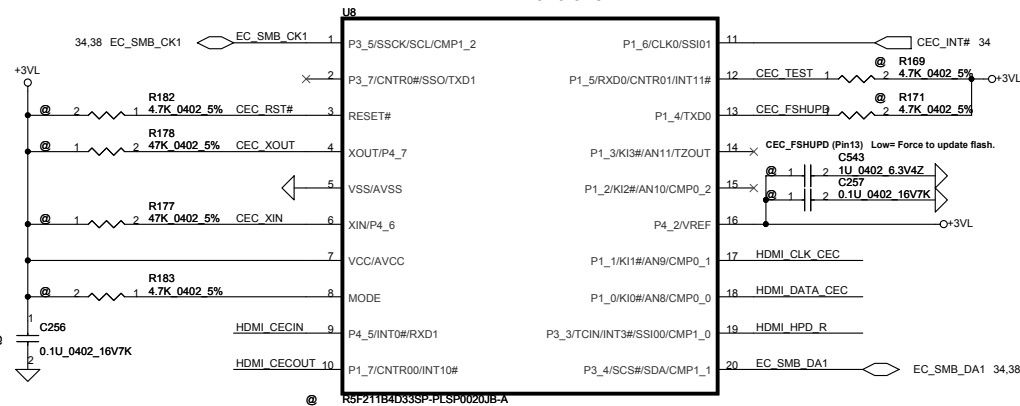
LCD/PANEL BD. Conn.



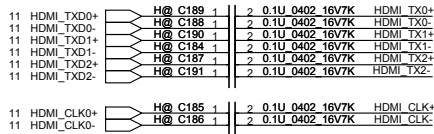
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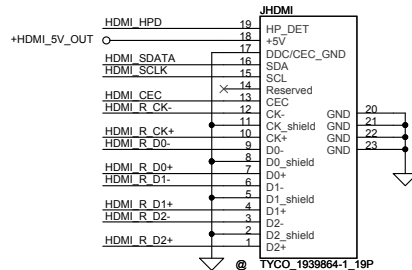
< HDMI CEC Controller >



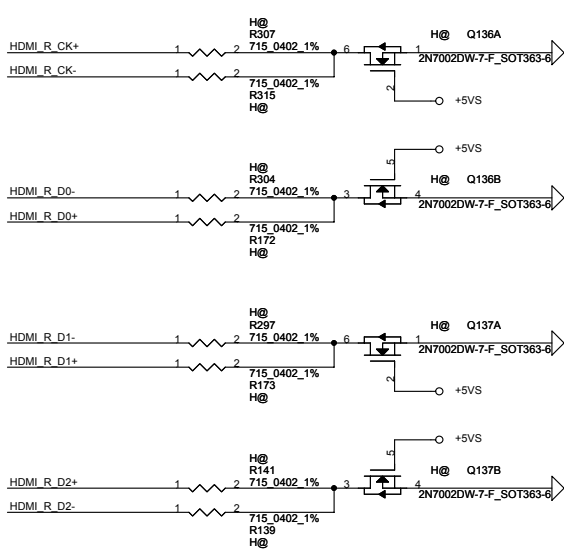
SI: Add R616~R624 for EMI request



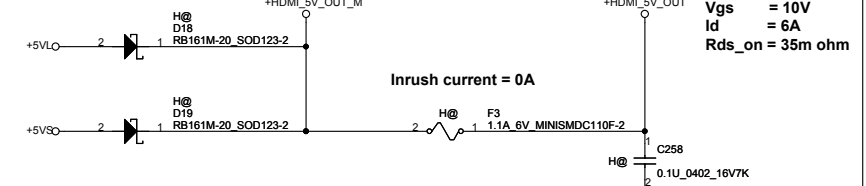
< HDMI Connector >



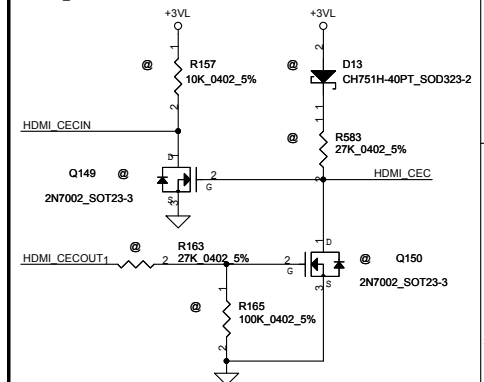
< Termination resistor >



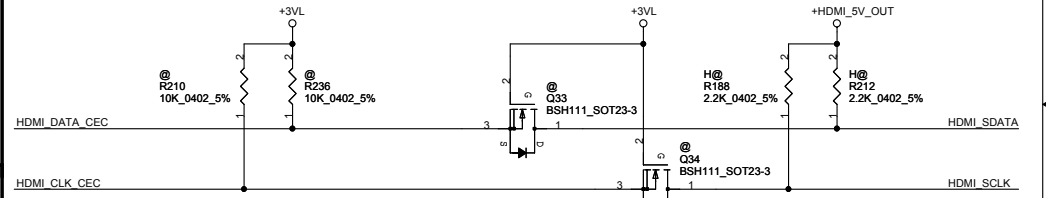
< Power, reset and crystal >



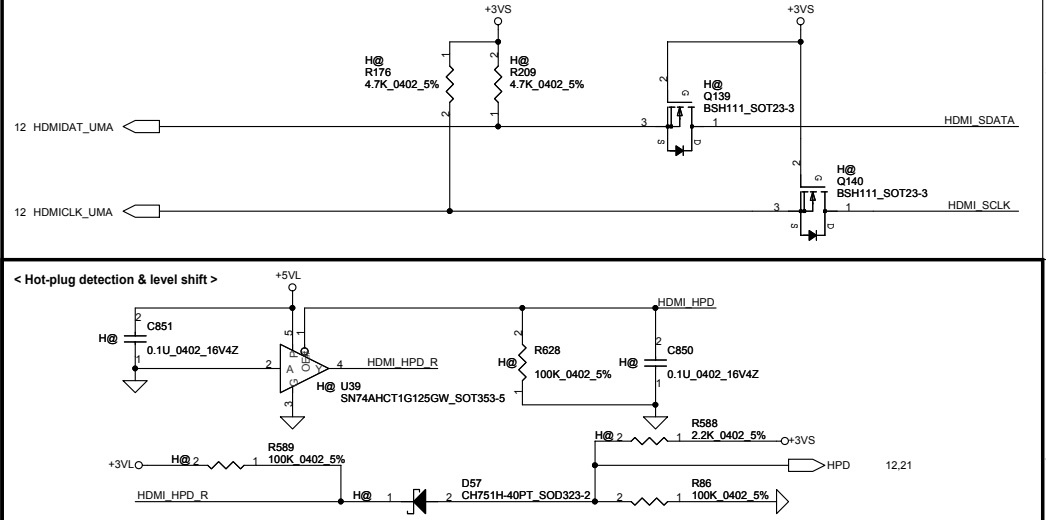
< HDMI_CEC level shift > < Place MOSFET close to HDMI connector >



< HDMI DDC channel to device >

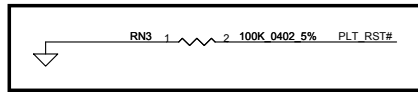


< Hot-plug detection & level shift >



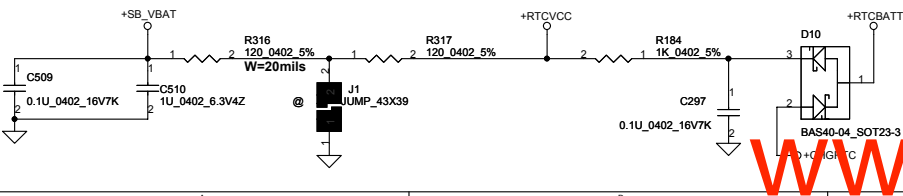
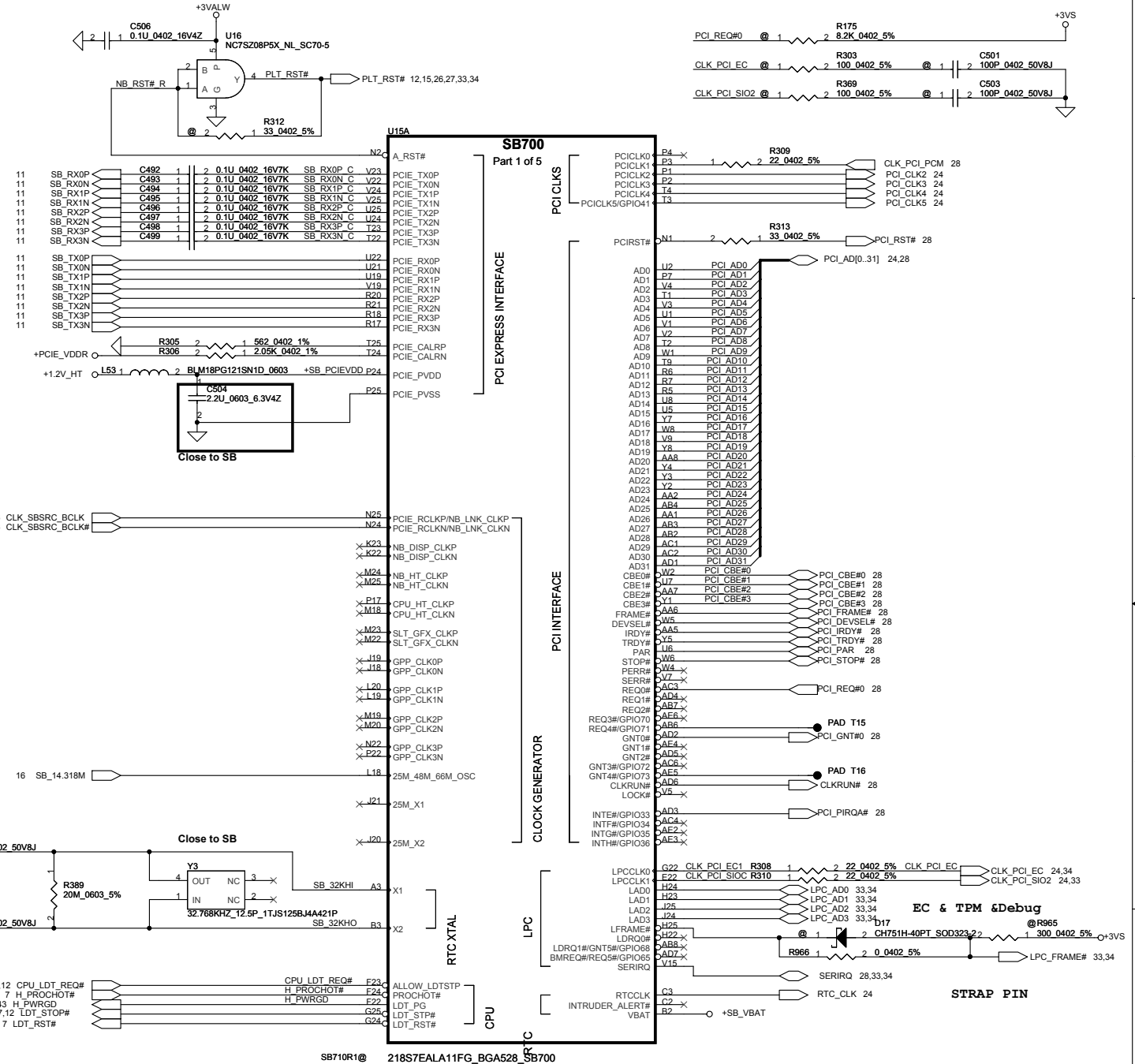
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< x4 PCIE A-link To NB >

< x4 PCIE A-link from NB >

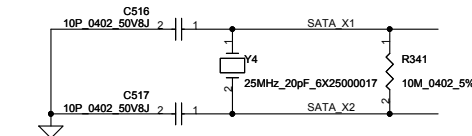
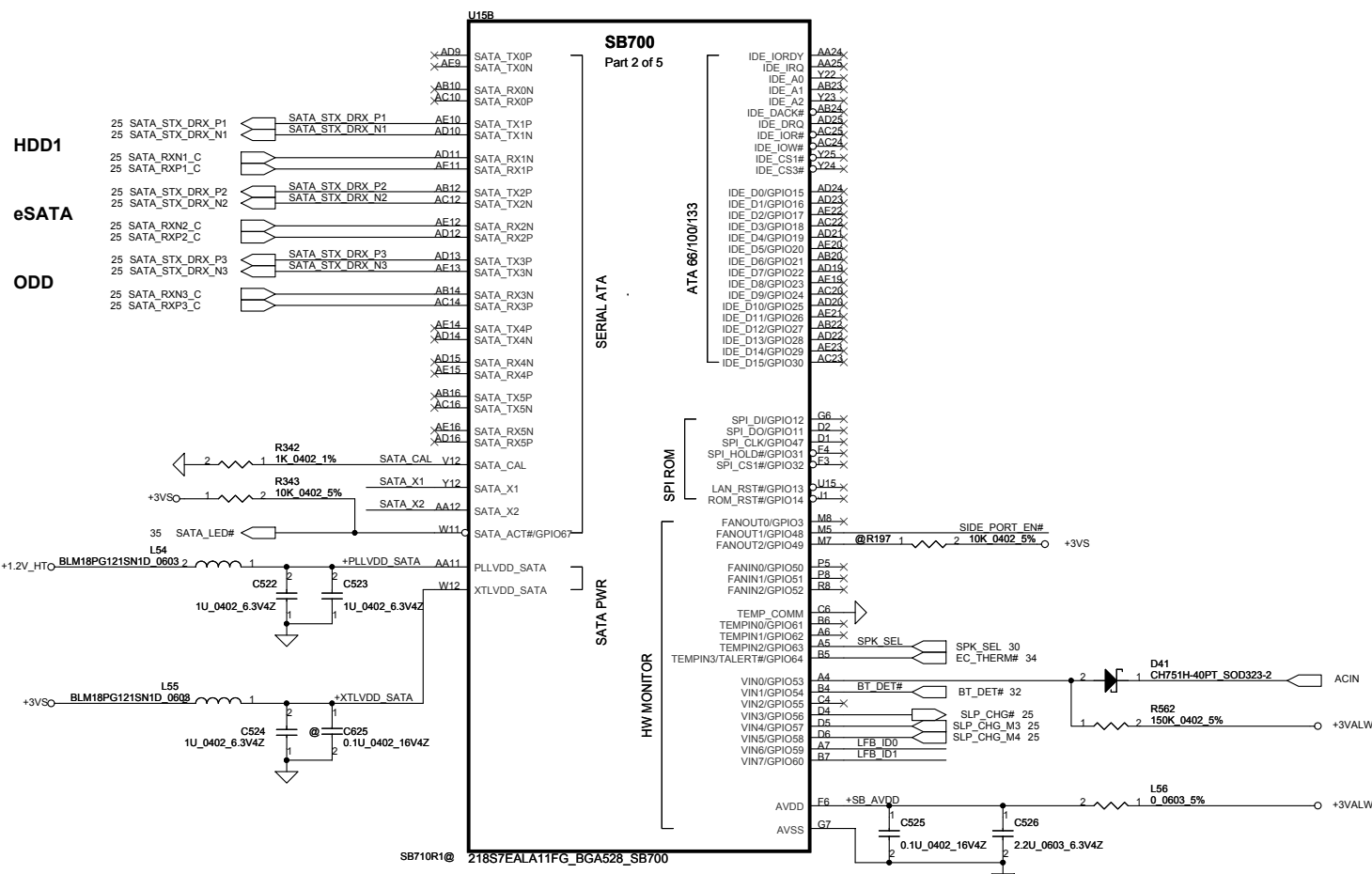


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HDD1

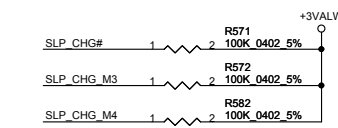
eSATA

ODD



	HDMI DISABLE	HDMI ENABLE
SIDE_PORT_EN#	0	1

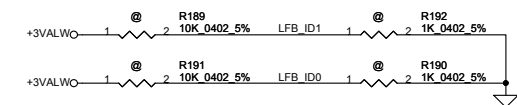
GPIO48,GPIO49 GOT INTERNAL PU 8.2K TO S0



	LFB_ID1	LFB_ID0
Hynix	0	0
Samsung	0	1
	1	0
	1	1

SA00002UH00 : Hynix
SA000031O00 : Samsung
64M*16 DDR2 500MHZ

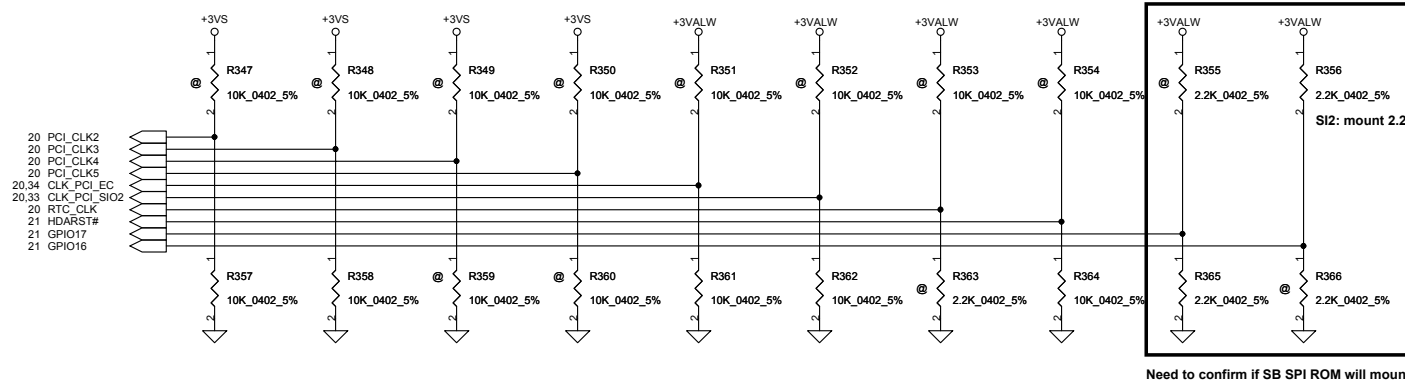
LFB_ID0 to LFB_ID1 got internal PU 10K to S5.



REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

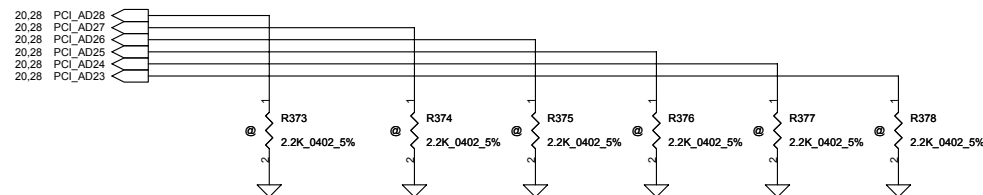
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM



DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

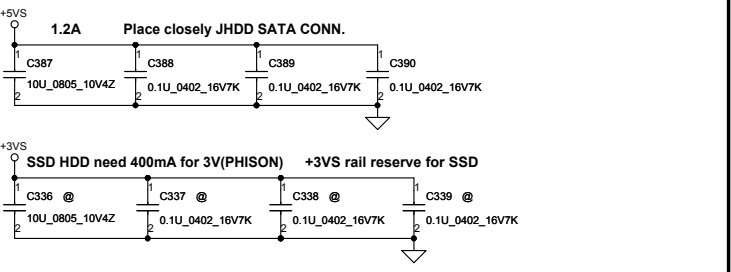
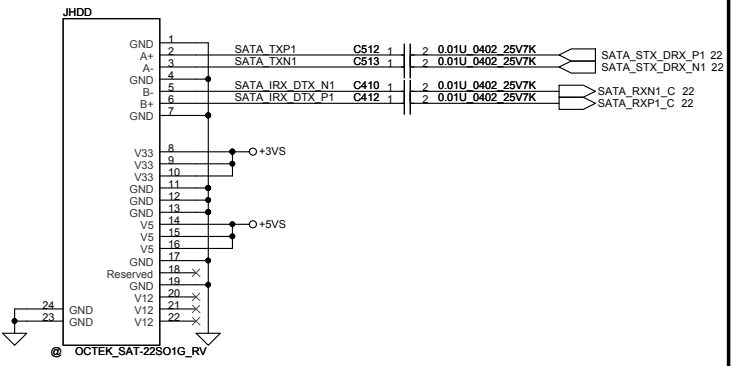
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	



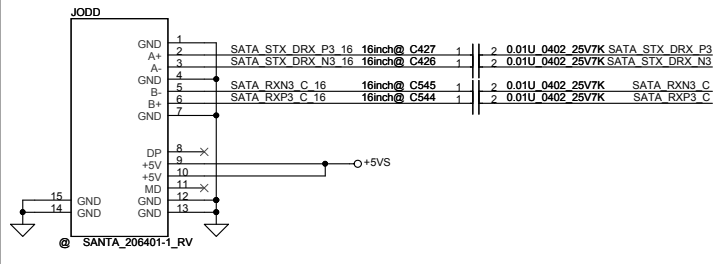
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
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				Size Custom	Document Number	Rev C
				401721		
				Date:	Wednesday, February 24, 2010	Sheet 24 of 45

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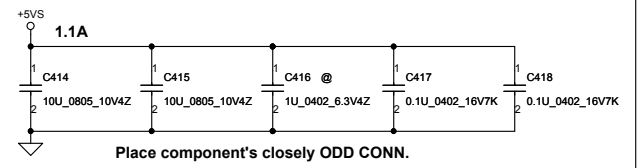
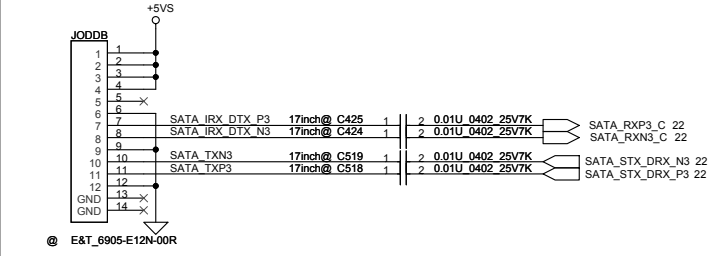
< SATA HDD1 Conn >



< 16" SATA ODD Conn >

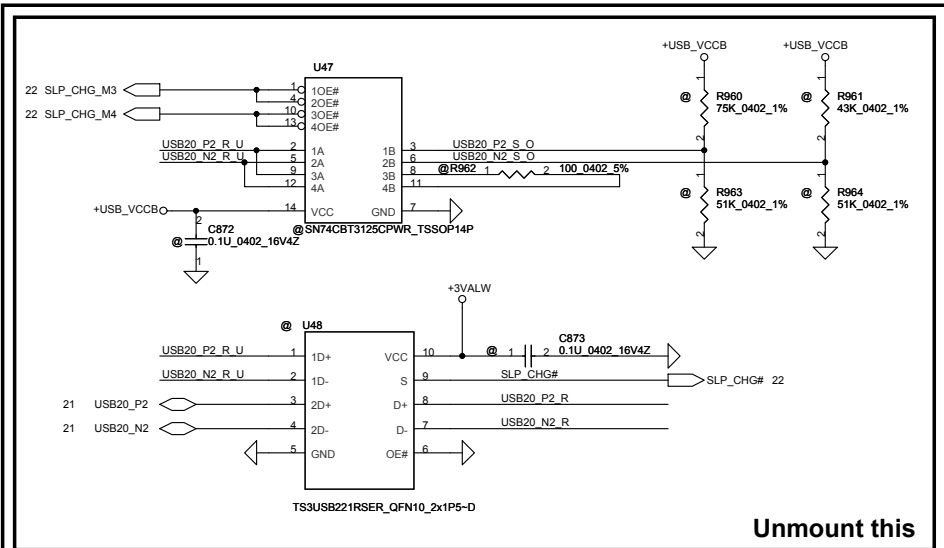


< 17" SATA ODD Conn >

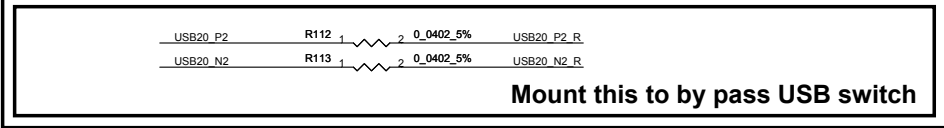


< eSATA/USB >

10/22 Add for USB Sleep & Charge M3/M4

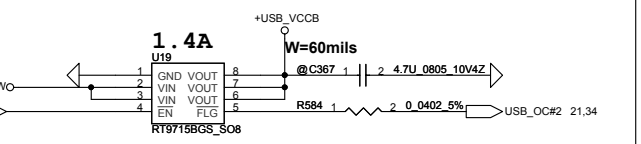
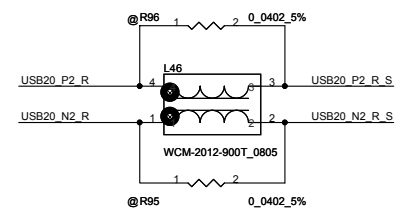


Unmount this

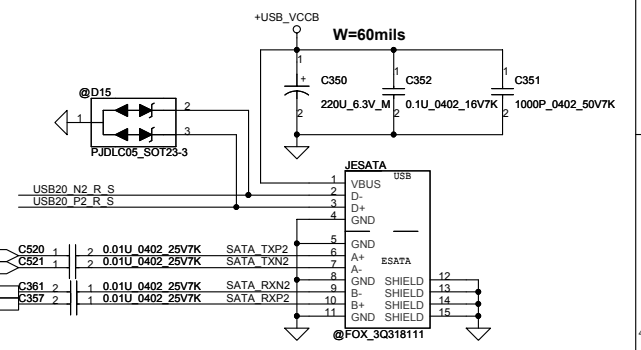


Mount this to by pass USB switch

Reserve for EMI request



eSATA/USB Conn



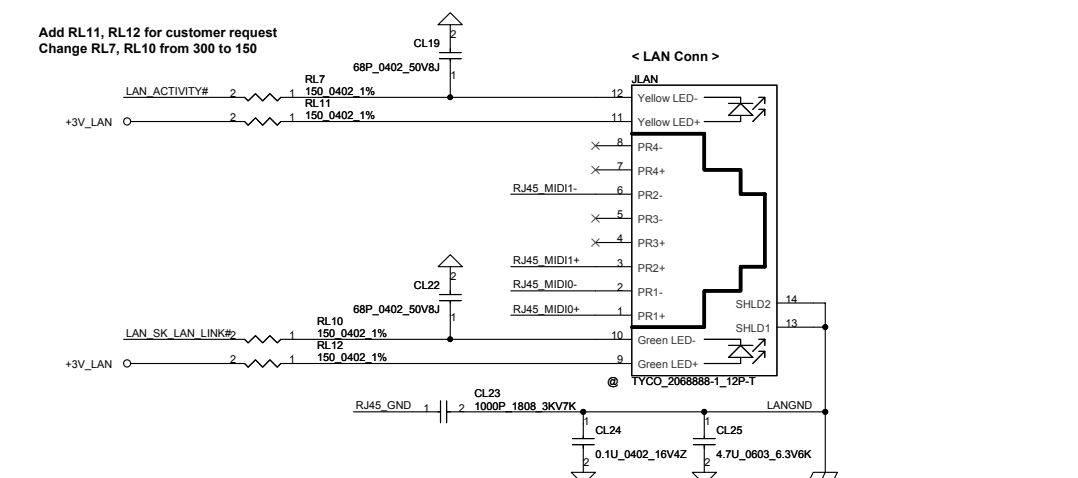
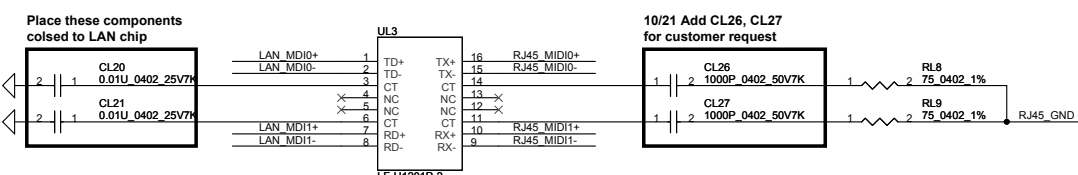
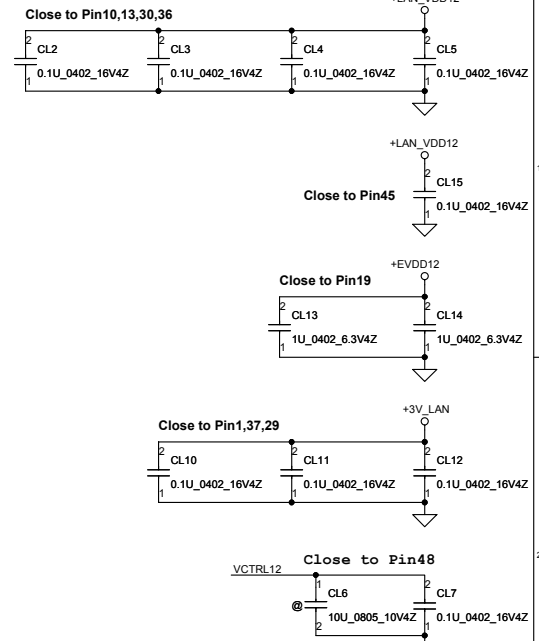
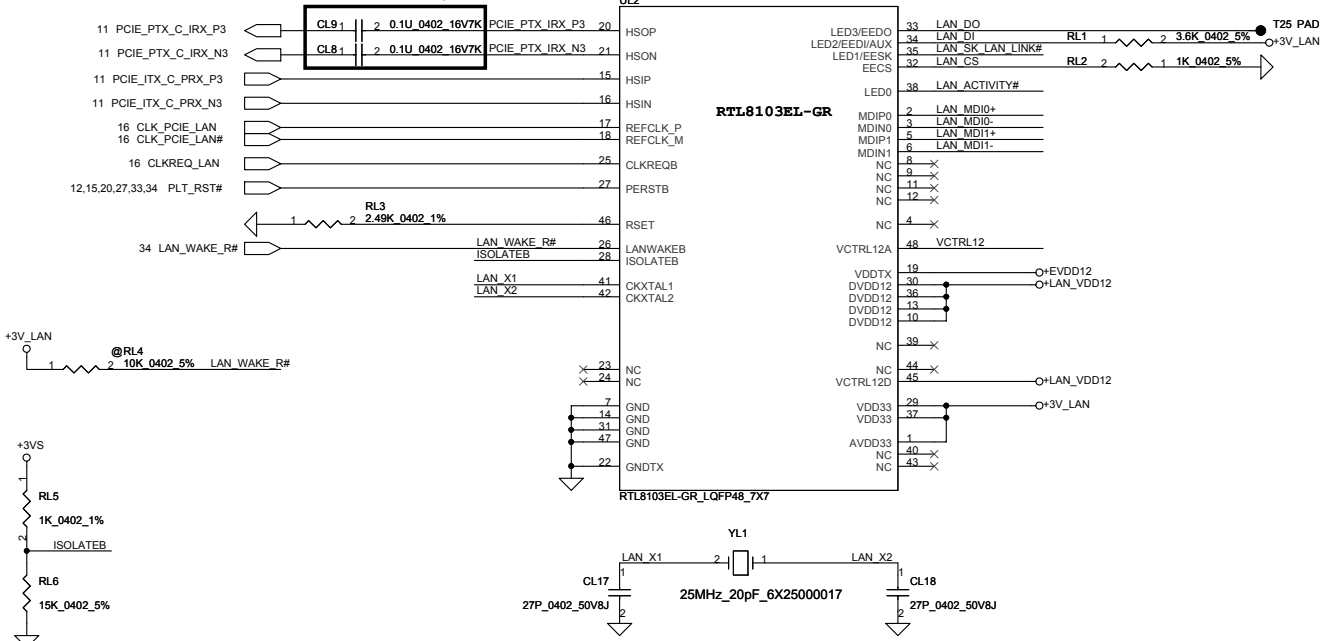
	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG#	FUNCTION
Mode 3	HIGH	LOW	LOW	D=1D
Mode 4	LOW	HIGH	HIGH	D=2D

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Date		Wednesday, February 24, 2010	

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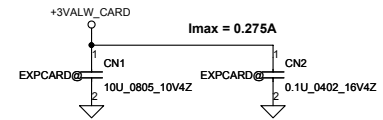
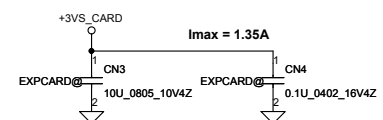
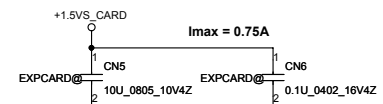
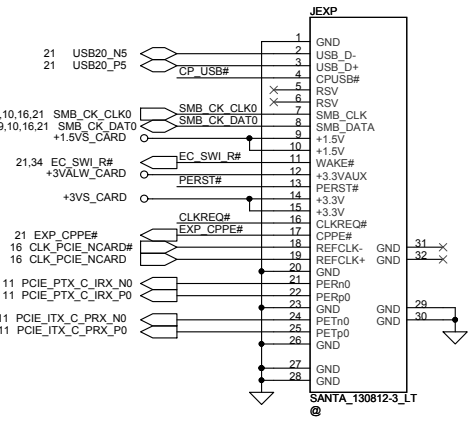
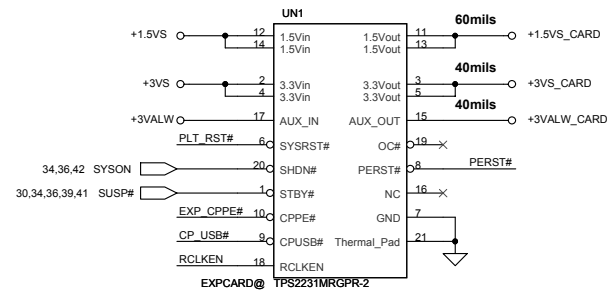
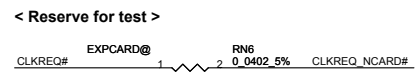
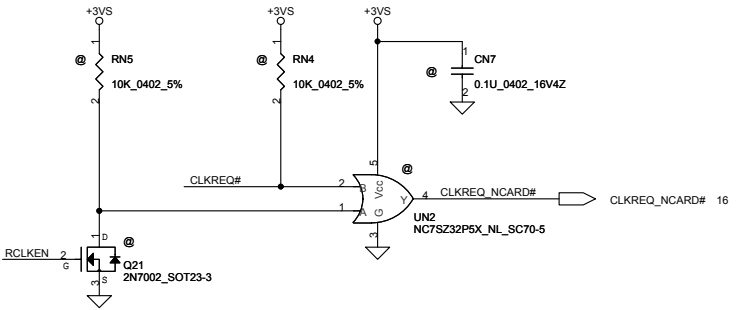
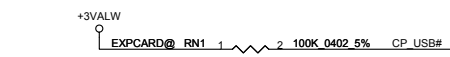
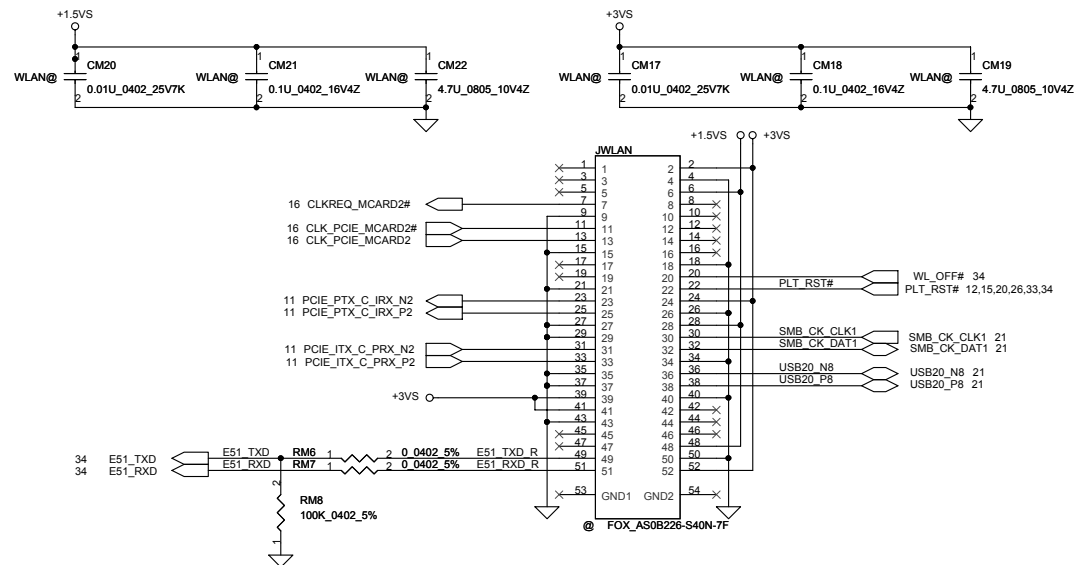
Place Close to Chip



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				Sheet	26 of 45
				Rev	C

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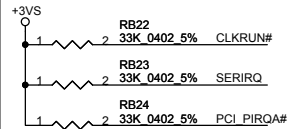
< PCIe Mini Card for WLAN >



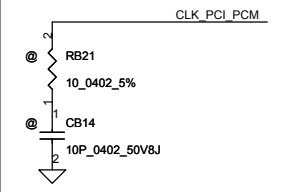
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22K TO 47K PULL-UPS MUST BE PLACED ON INTA#, PME#, SERIRQ# & CLKRUN#.



For EMI



NOTE: IDSEL SELECTION!

THIS DEVICE UTILIZES A "SELECTABLE IDSEL" SCHEME.

IDSEL CAN BE CONNECTED INTERNALLY TO ONE OF THREE PCI AD LINES OR EXTERNAL IDSEL SIGNAL.

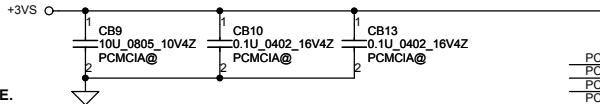
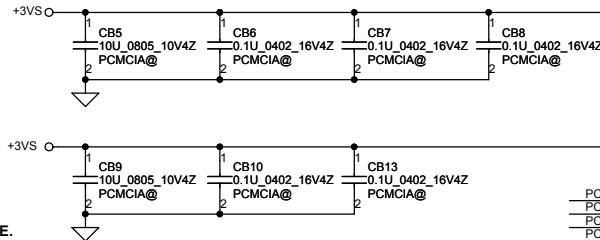
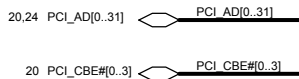
22K TO 47K PULL-UP & PULL-DOWN RESISTORS ARE REQUIRED TO BE CONNECTED TO PINS 123 & 124 TO SELECT ONE OF THE 4 POSSIBLE IDSEL CONNECTIONS.

THE TABLE BELOW SHOWS THE 4 POSSIBLE COMBINATIONS.

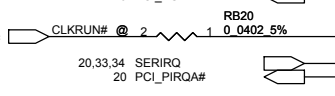
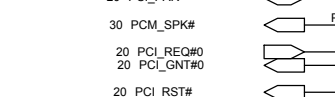
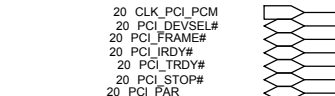
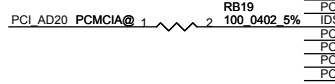
CONFIGURING IDSEL TO BE INTERNALLY CONNECTED ALLOWS FOR A FULL PARALLEL POWER MODE. IF AN EXTERNALLY CONNECTED IDSEL IS REQUIRED THEN AN INVERTER MUST BE CONNECTED TO VPP_PGM TO CREATE VPP_VCC.

VCC5# (124)	VPP_PGM (123)	IDSEL SELECT
DOWN	DOWN	AD18
DOWN	UP	AD20
UP	DOWN	AD25
UP	UP	PIN 127 ball F4

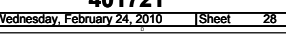
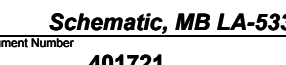
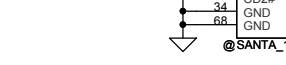
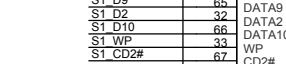
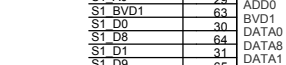
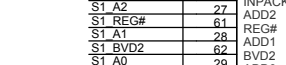
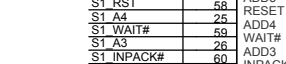
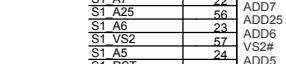
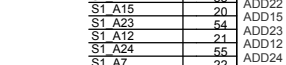
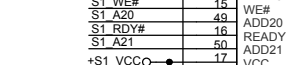
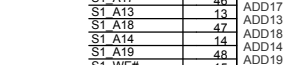
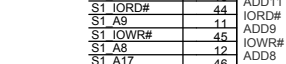
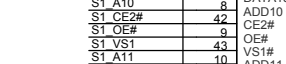
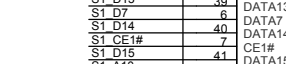
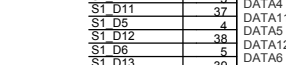
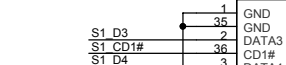
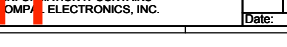
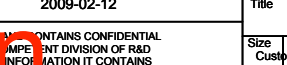
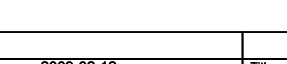
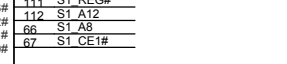
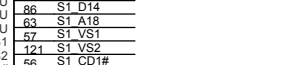
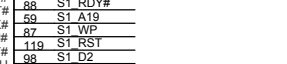
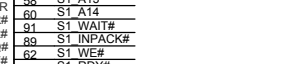
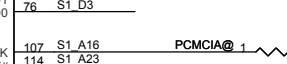
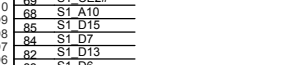
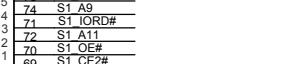
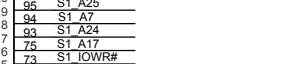
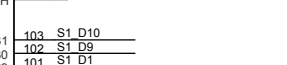
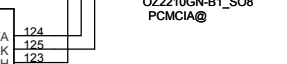
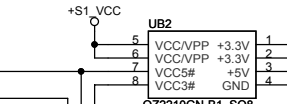
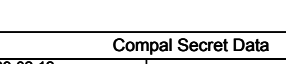
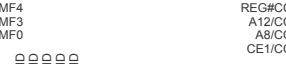
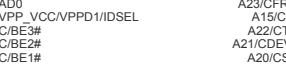
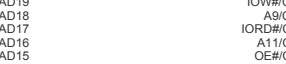
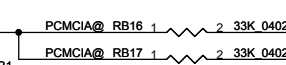
must check IDSEL, PCI_PIRQ#,



PCI AD31	4	AD31
PCI AD30	5	AD30
PCI AD29	6	AD29
PCI AD28	7	AD28
PCI AD27	8	AD27
PCI AD26	9	AD26
PCI AD25	10	AD25
PCI AD24	11	AD24
PCI AD23	12	AD23
PCI AD22	13	AD22
PCI AD21	14	AD21
PCI AD20	15	AD20
PCI AD19	16	AD19
PCI AD18	17	AD18
PCI AD17	18	AD17
PCI AD16	19	AD16
PCI AD15	20	AD15
PCI AD14	21	AD14
PCI AD13	22	AD13
PCI AD12	23	AD12
PCI AD11	24	AD11
PCI AD10	25	AD10
PCI AD9	26	AD9
PCI AD8	27	AD8
PCI AD7	28	AD7
PCI AD6	29	AD6
PCI AD5	30	AD5
PCI AD4	31	AD4
PCI AD3	32	AD3
PCI AD2	33	AD2
PCI AD1	34	AD1
PCI AD0	35	AD0
IDSEL	127	VPP_VCC/VPPD1/IDSEL
PCI_CBE#3	11	C/BE3#
PCI_CBE#2	12	C/BE2#
PCI_CBE#1	13	C/BE1#
PCI_CBE#0	14	C/BE0#

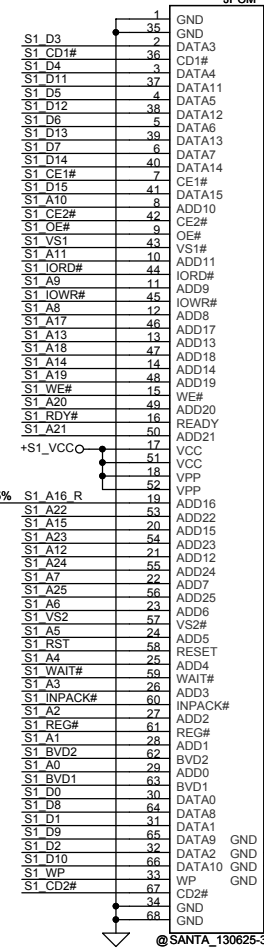


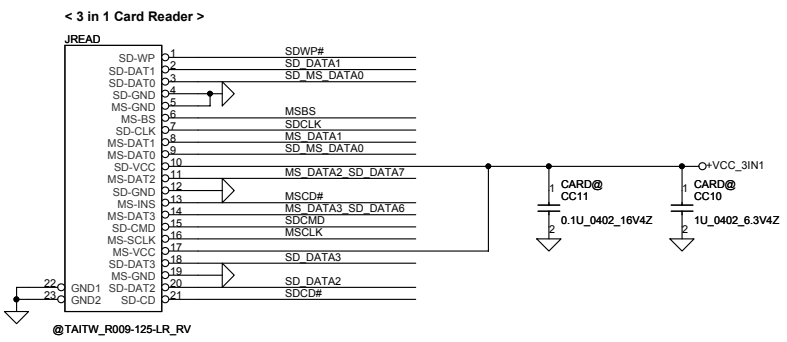
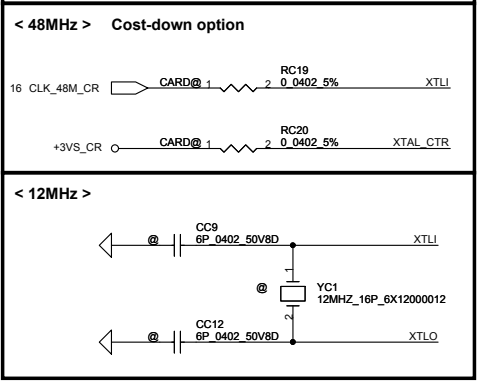
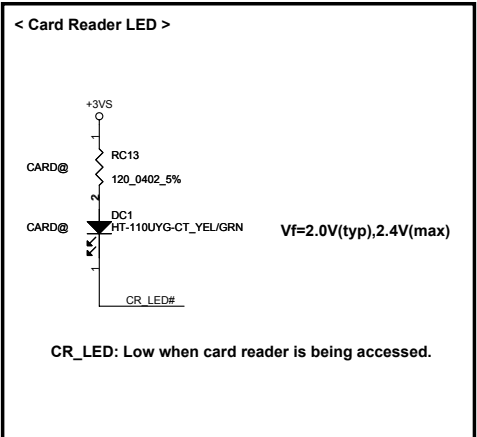
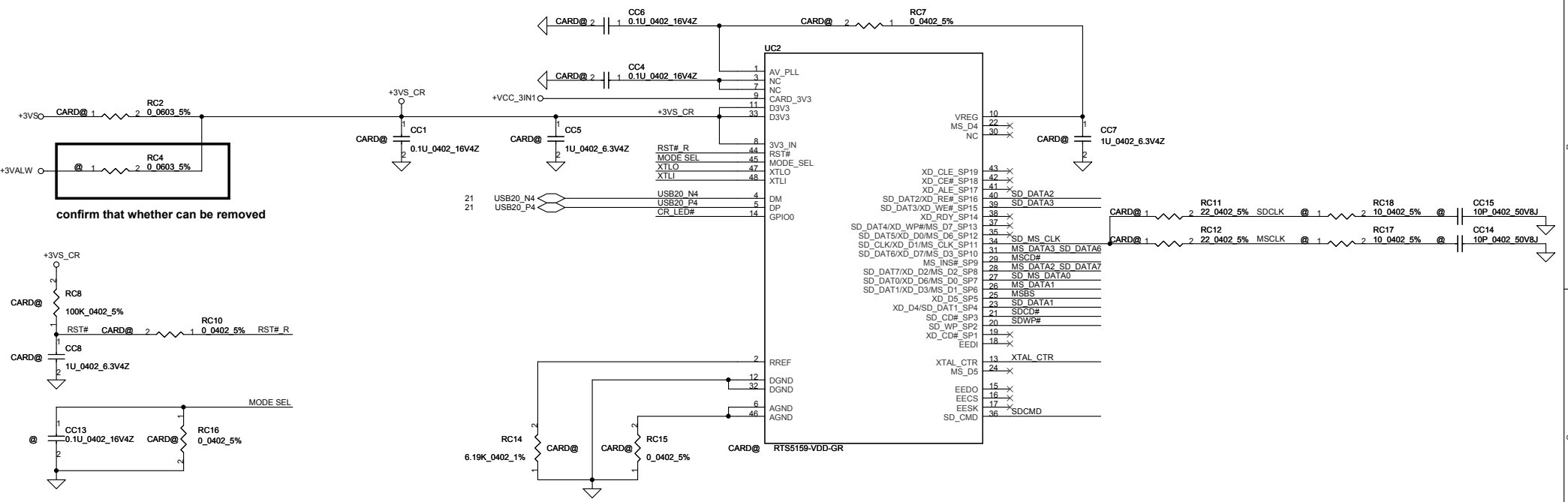
IDSEL SELECT POWER-ON-STRAPPING
(SEE NOTE & TABLE FOR OPTIONS)



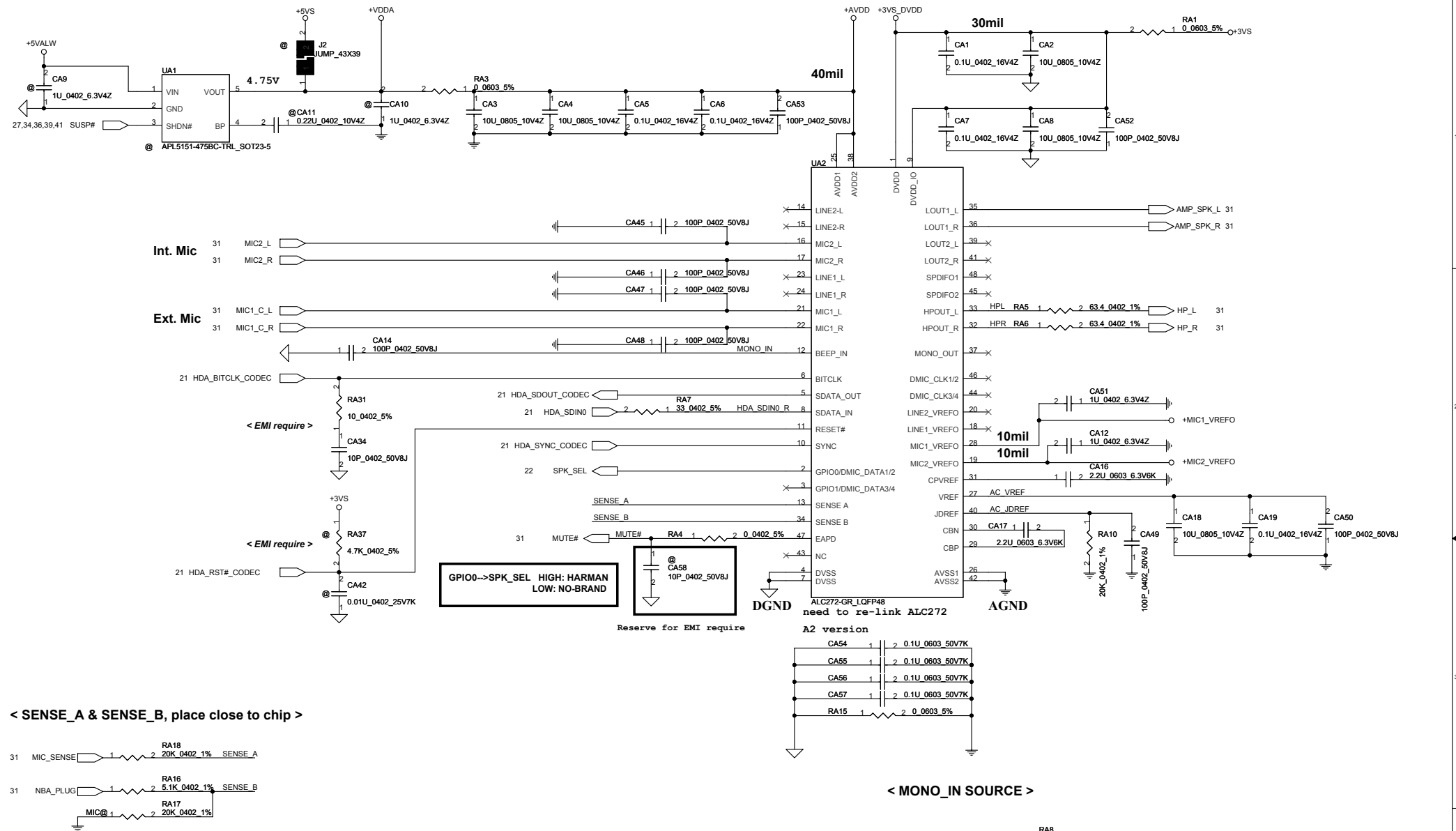
PCMCIA Socket

JPCM





R	C	USB AUTO DE-LINK	MS FORMATTER	Description
0	NC	YES		Recommended
NC	47P	YES	YES	
NC	NC			Compatible with RTS5158E
NC	680P	YES		LED ON
10K	180P			LED ON
10K	680P		YES	

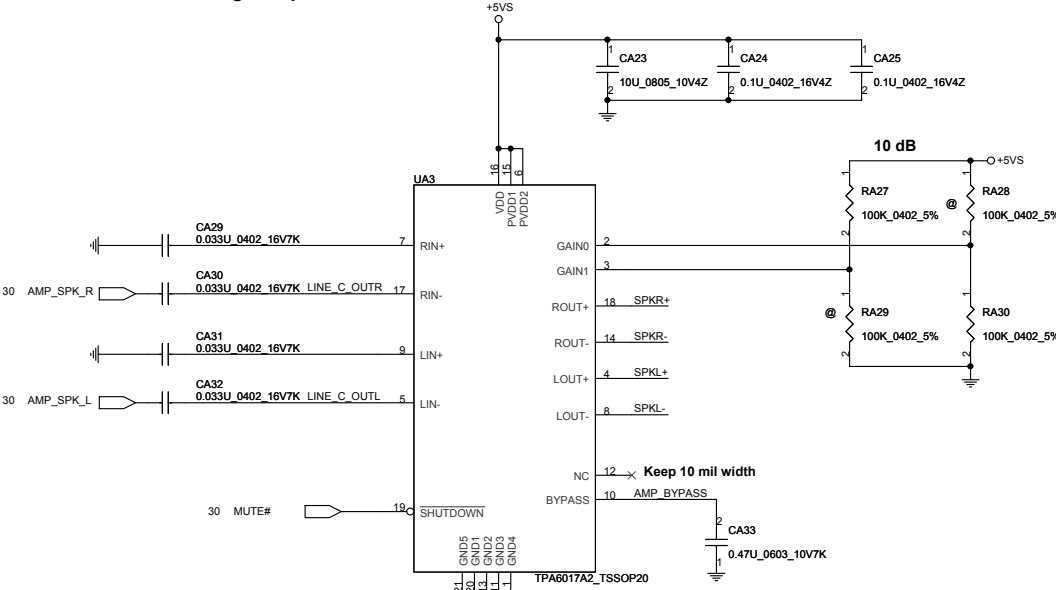


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	SPK out
SENSE B	39.2K	PORT-E (PIN 14, 15)	Int. MIC
	20K	PORT-F (PIN 16, 17)	
	10K	PORT-H (PIN 37)	Headphone out
	5.1K	PORT-I (PIN 32, 33)	

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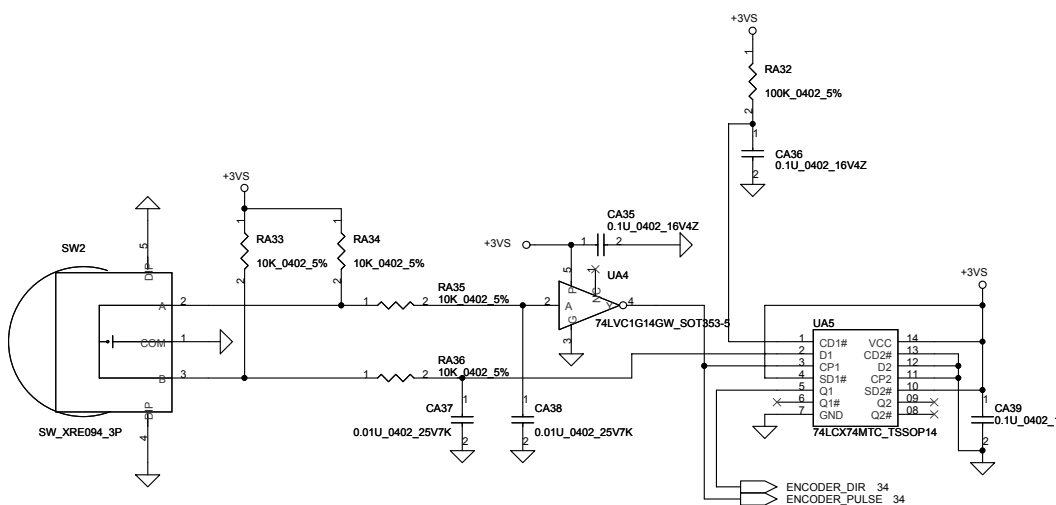
www.vinfix.vn

< TPA6017 Medium Range Amplifier >

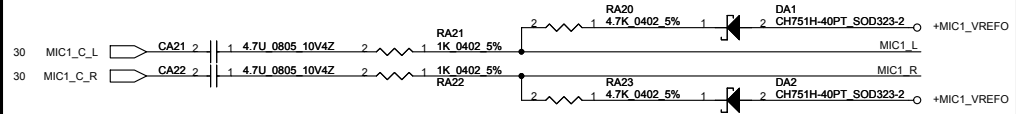


GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

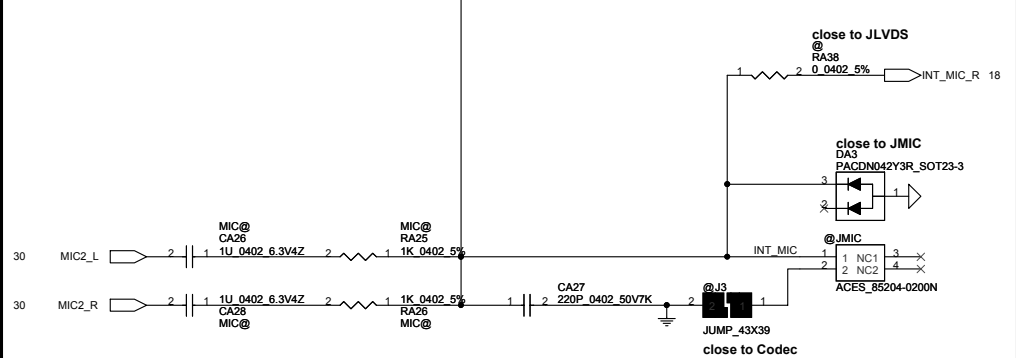
< Volume Control >



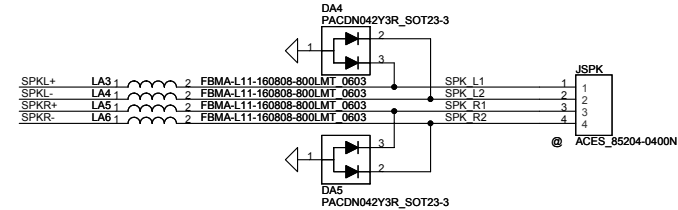
< Ext. Mic >



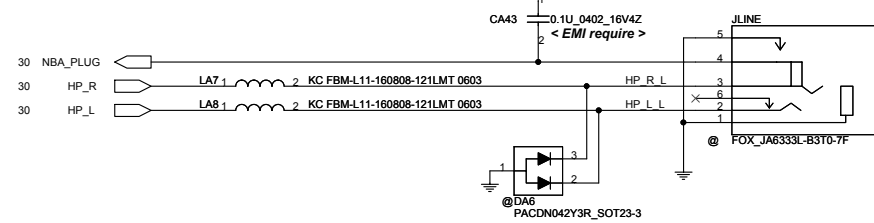
< Int. Mic >



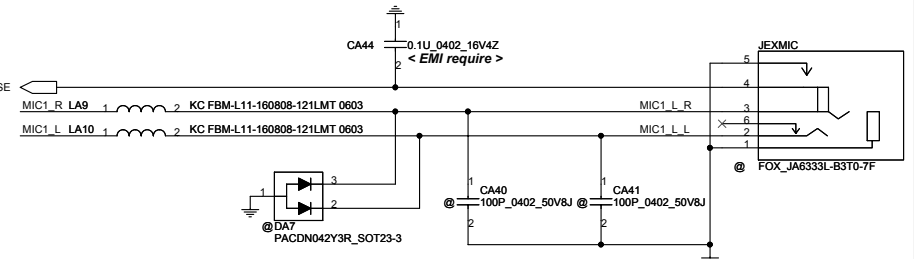
< Speaker Connector >



< HeadPhone JACK >



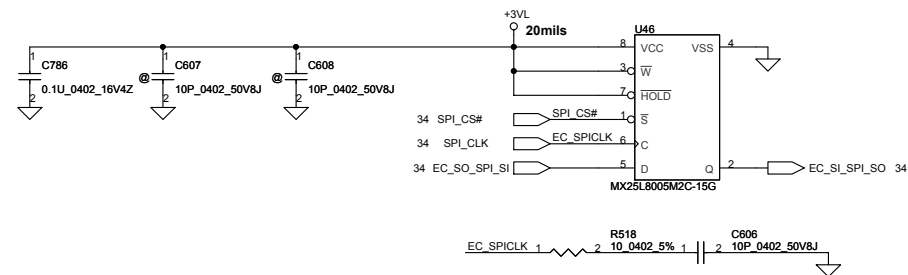
< Ext.MIC/LINE IN JACK >



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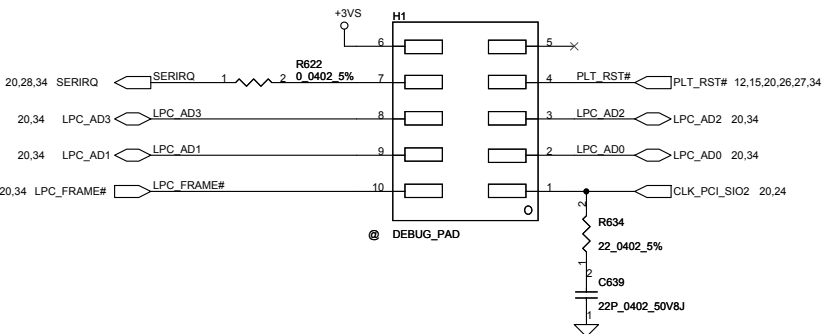
www.winfix.vn

< SPI Flash 8Mb*1 >

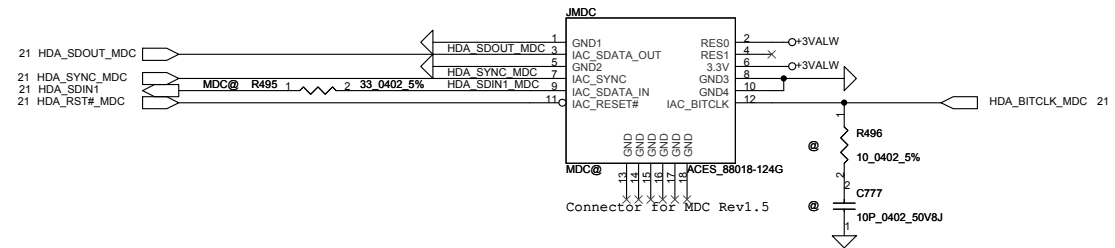


< LPC Debug Port >

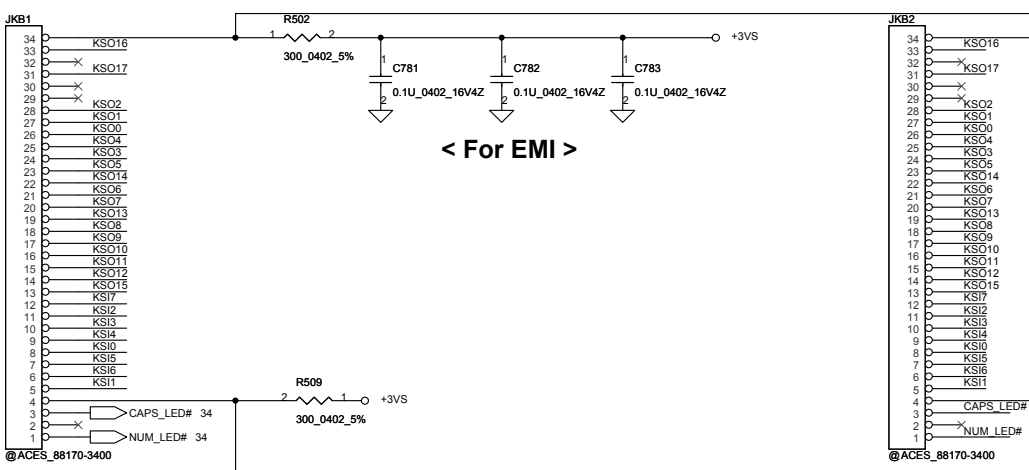
Please place the PAD under DDR DIMM.



< MDC 1.5 Conn >

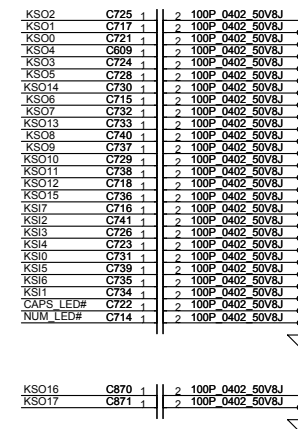


< KEYBOARD CONN 16" >



< KEYBOARD CONN 17" >

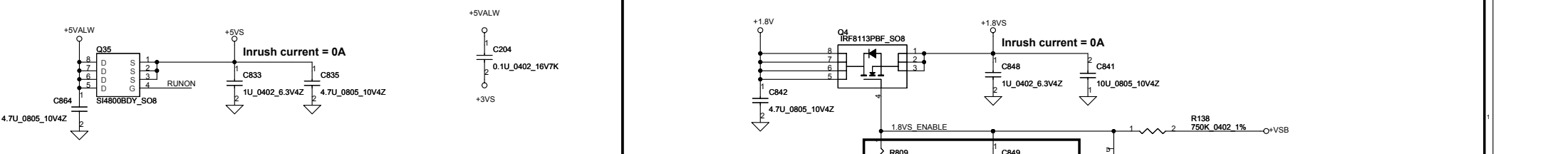
< For EMI >



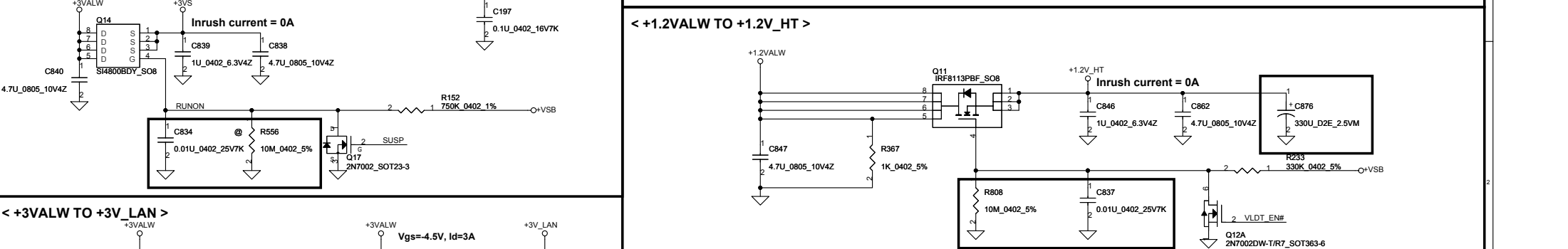
KSI[0..7] KSI[0..7] 34,35
KSO[0..17] KSO[0..17] 34,35

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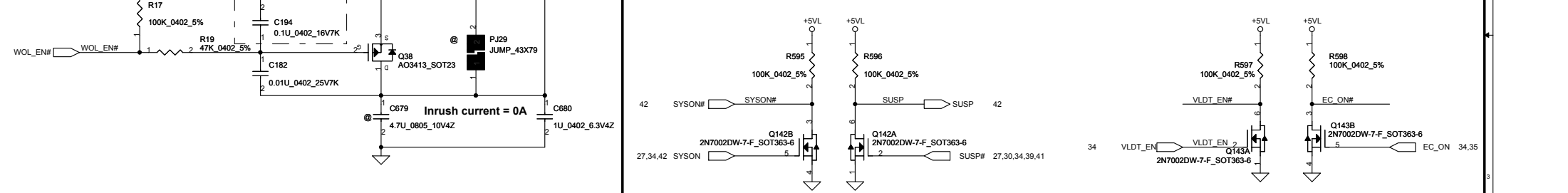
< +5VALW TO +5VS > < close to PQ20, must EMI confirm > < +1.8V TO +1.8VS >



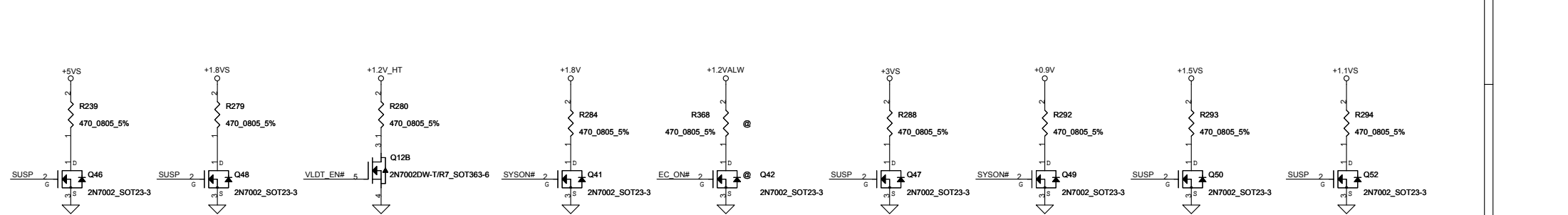
< +3VALW TO +3VS > < close to PQ20, must EMI confirm > < +1.2VALW TO +1.2V_HT >



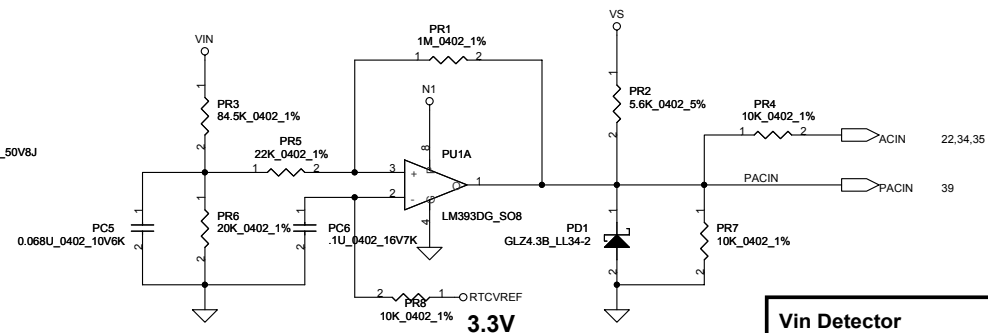
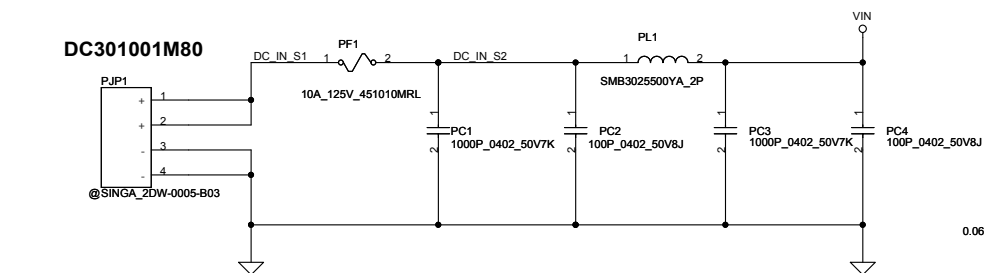
< +3VALW TO +3V_LAN > < Inversion of SYSON, SUSP#, VLDT_EN, EC_ON >



< Discharge circuit >

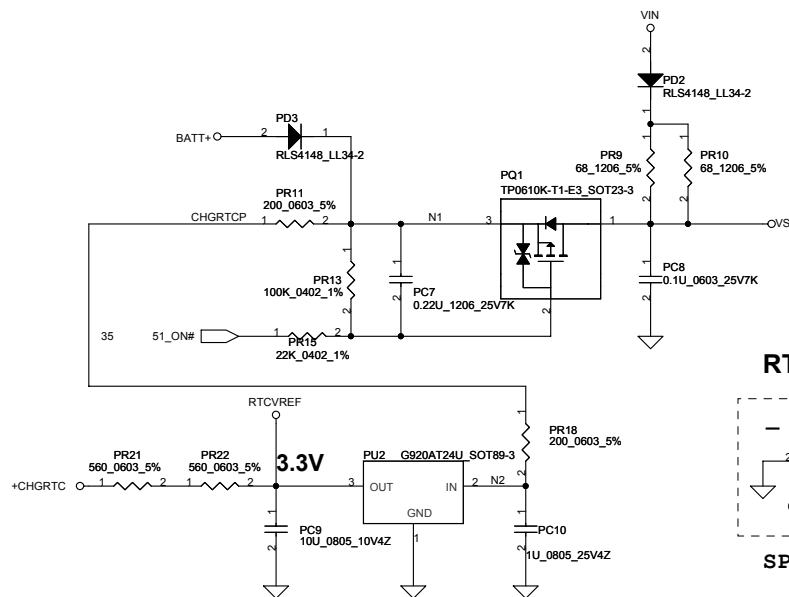


DC301001M80

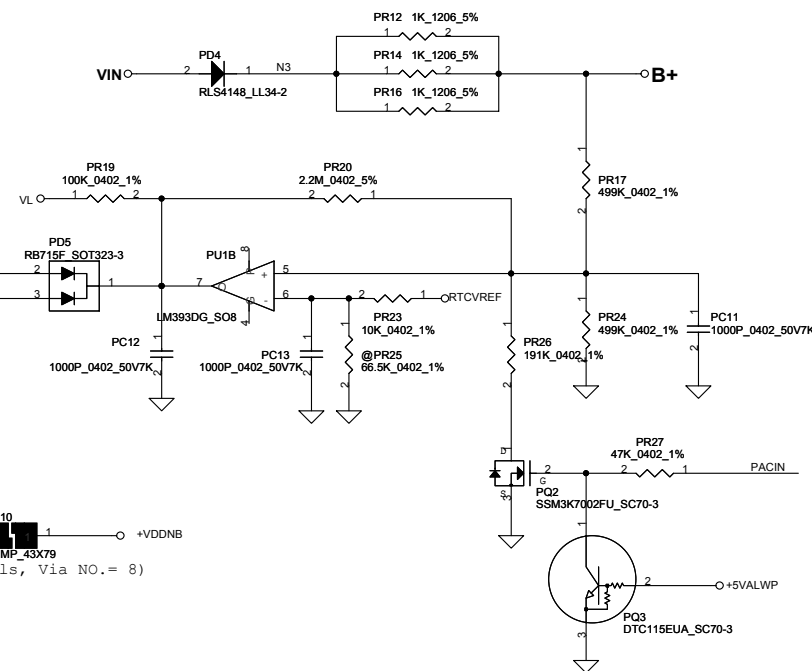
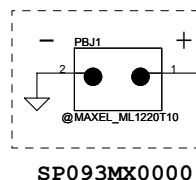


Vin Detector

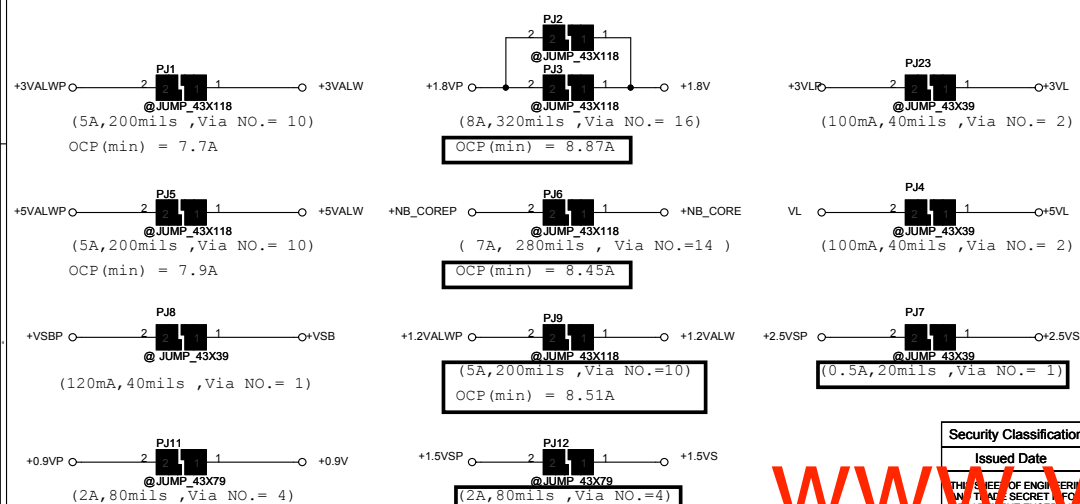
High 18.384 17.901 17.430
Low 17.728 17.257 16.976



RTC Battery



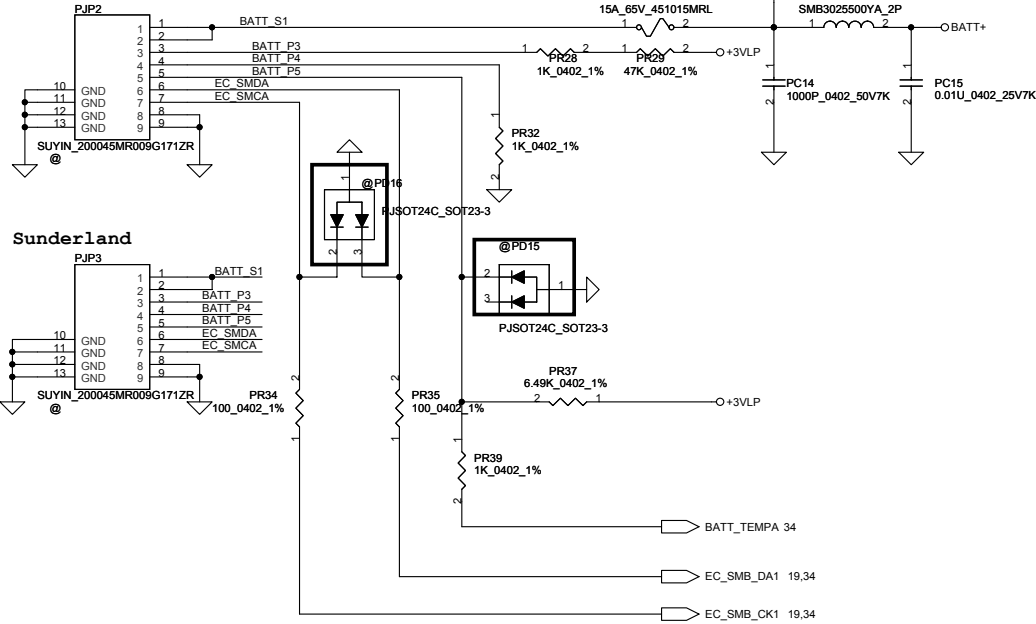
Precharge detector 15.97V/14.84V FOR ADAPTOR



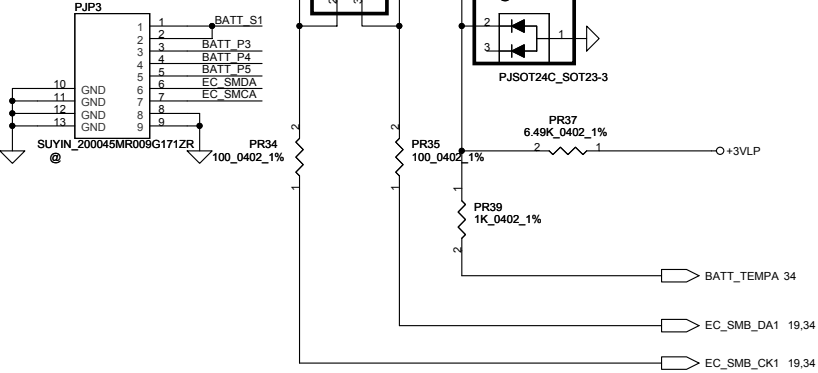
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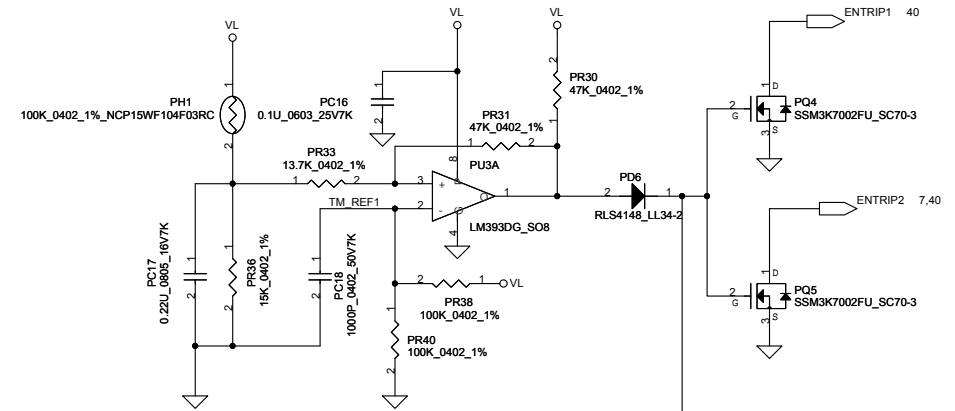
Liverpool



Sunderland

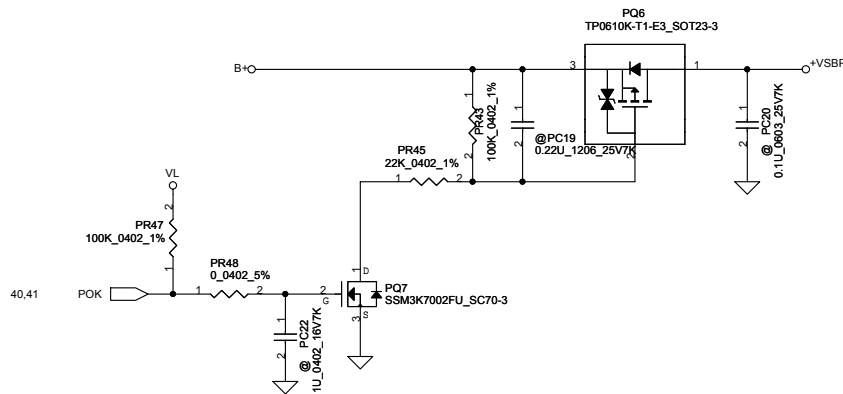
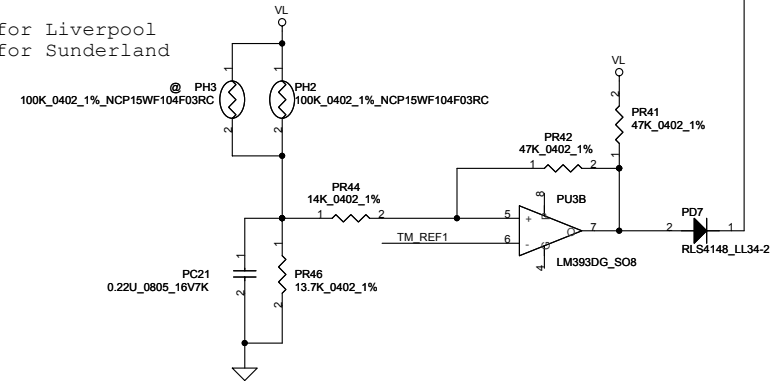


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 57 degree C

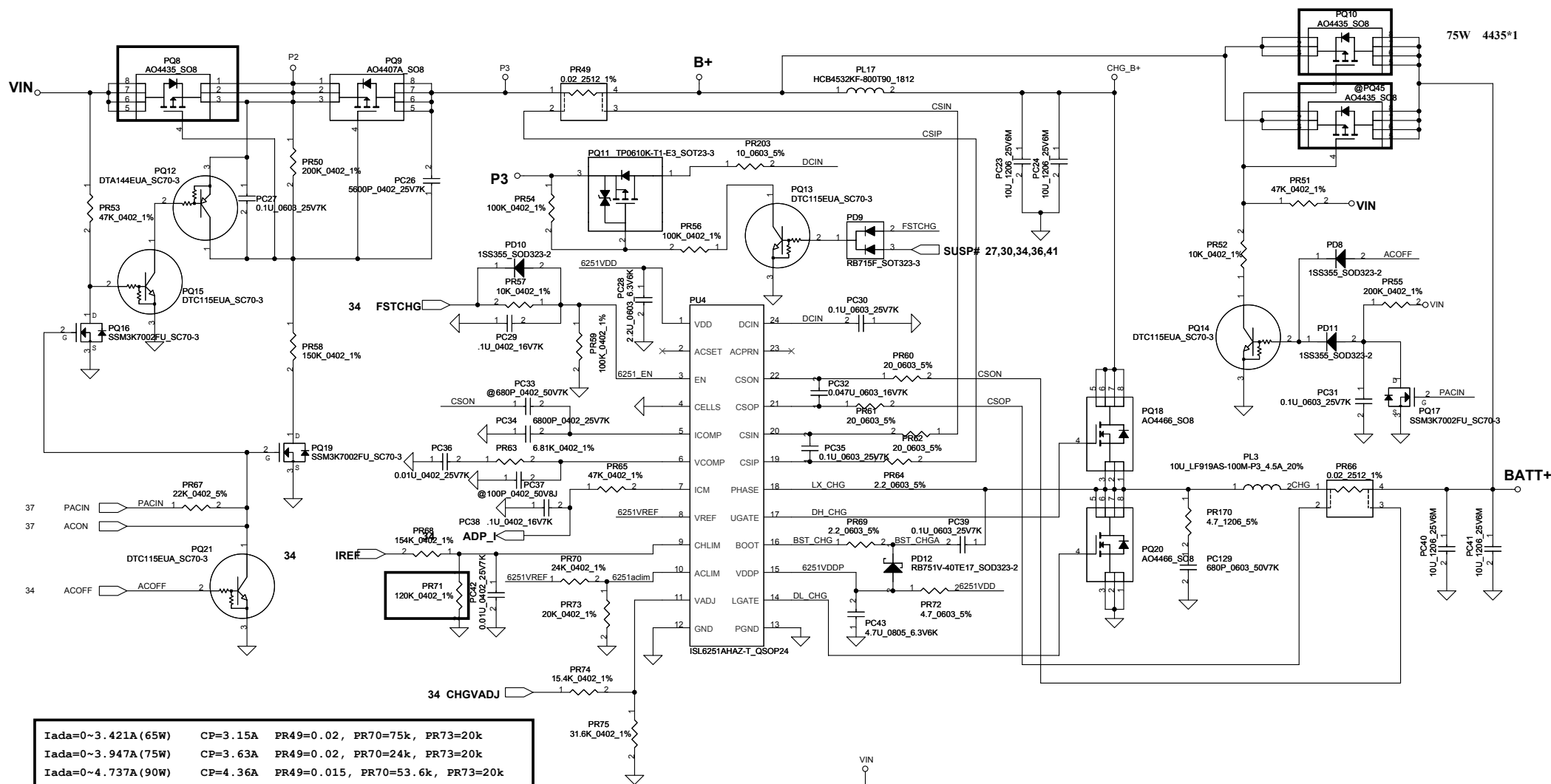


PH2 near main Battery CONN :
BAT. thermal protection at 98 degree C
Recovery at 60 degree C

PH2 for Liverpool
PH3 for Sunderland



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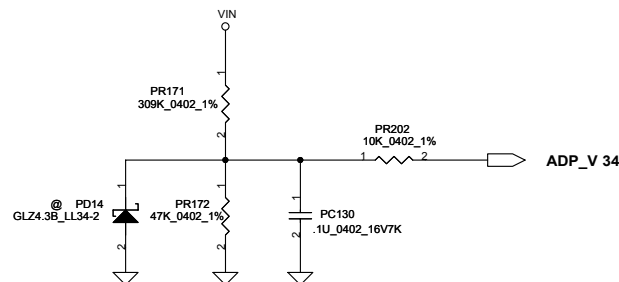


$I_{ada} = 0 \sim 3.421A (65W)$ $CP = 3.15A$ $PR49 = 0.02, PR70 = 75k, PR73 = 20k$
 $I_{ada} = 0 \sim 3.947A (75W)$ $CP = 3.63A$ $PR49 = 0.02, PR70 = 24k, PR73 = 20k$
 $I_{ada} = 0 \sim 4.737A (90W)$ $CP = 4.36A$ $PR49 = 0.015, PR70 = 53.6k, PR73 = 20k$
 $I_{ada} = 0 \sim 6.316A (120W)$ $CP = 5.81A$ $PR49 = 0.015, PR70 = 8.25k, PR73 = 26.7k$
 $CP = 92\% \cdot I_{ada}$

CP mode
 $V_{acim} = 2.39 \cdot (R_b / (152K) + (R_t / (152K + R_b) / (152K)))$
 $I_{input} = (1 / PR49) \cdot ((0.05 \cdot V_{acim}) / (2.39 + 0.05))$
 where $V_{acim} = 1.09986V, I_{input} = 3.65A$
 $V_{acim} = 0.7717V, I_{input} = 4.41A$
 $V_{acim} = 0.4204V, I_{input} = 5.88A$

CC=0.25A~3A		CHGVADJ=(Vcell-4)/0.10627	
IREF=1.016*Icharge		Vcell	CHGVADJ
IREF=0.254V~3.048V		4V	0V
VCHLIM need over 95mV		4.2V	1.882V
		4.35V	3.2935V

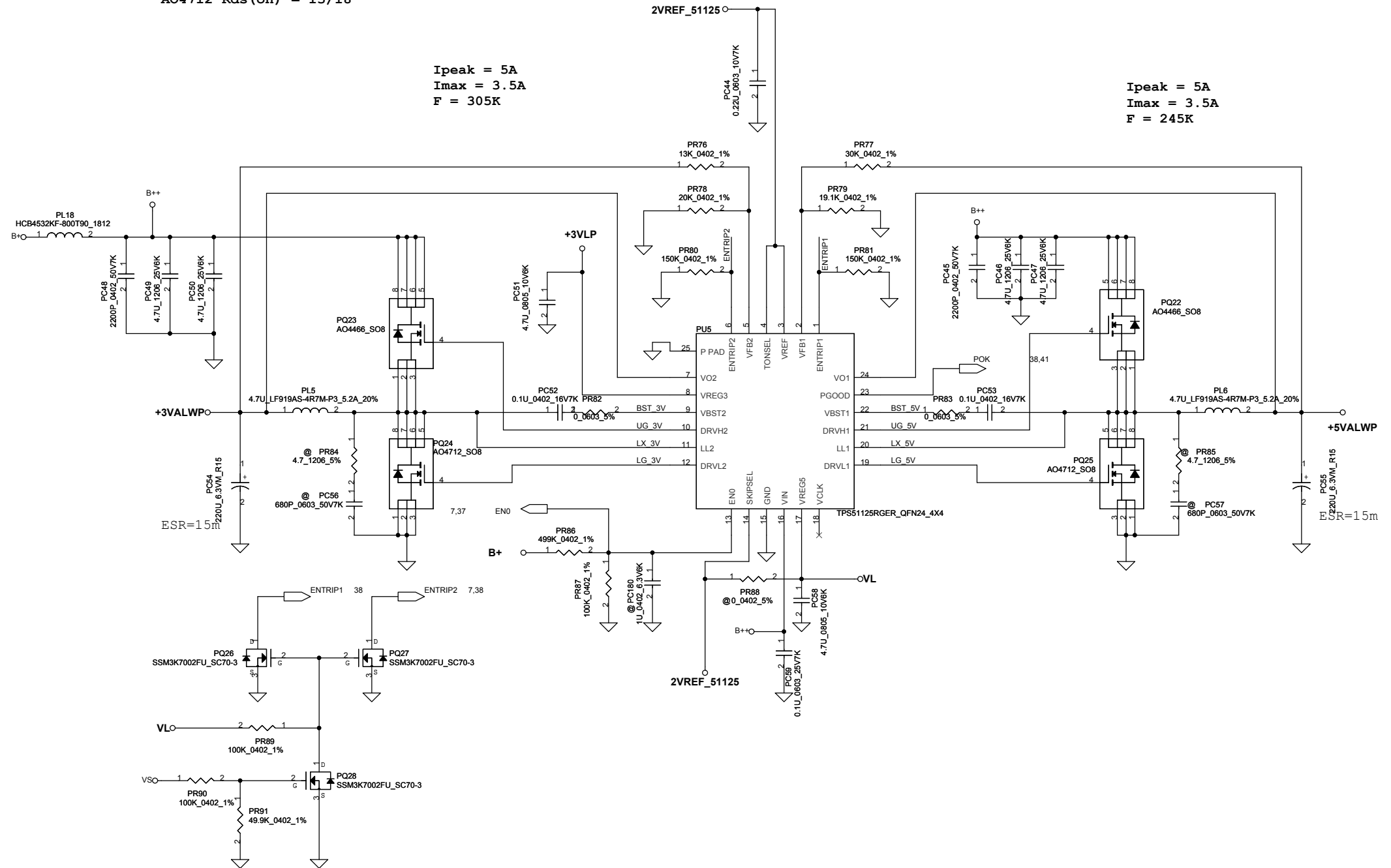
CELLS	VDD	GND	Float
CELL number	4	3	2



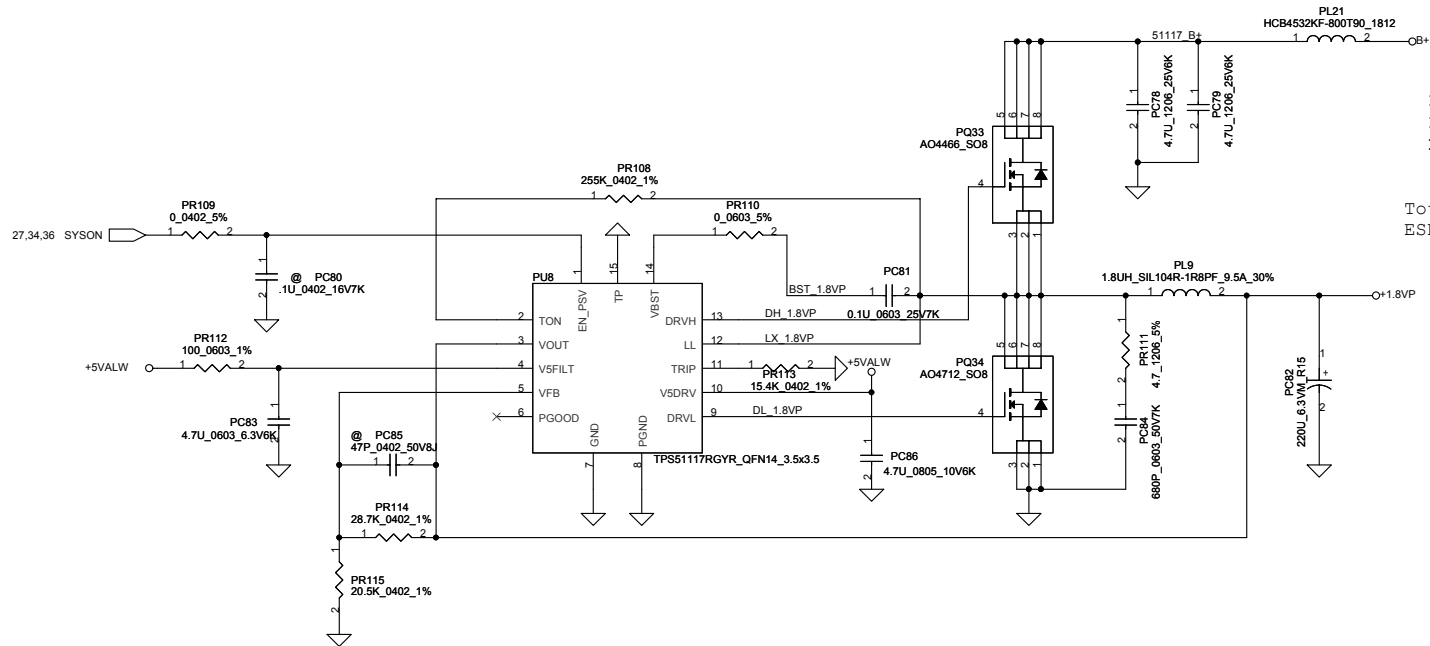
AO4712 Rds(on) = 15/18

I_{peak} = 5A
I_{max} = 3.5A
F = 305K

I_{peak} = 5A
I_{max} = 3.5A
F = 245K

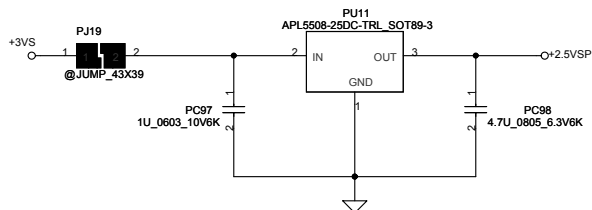
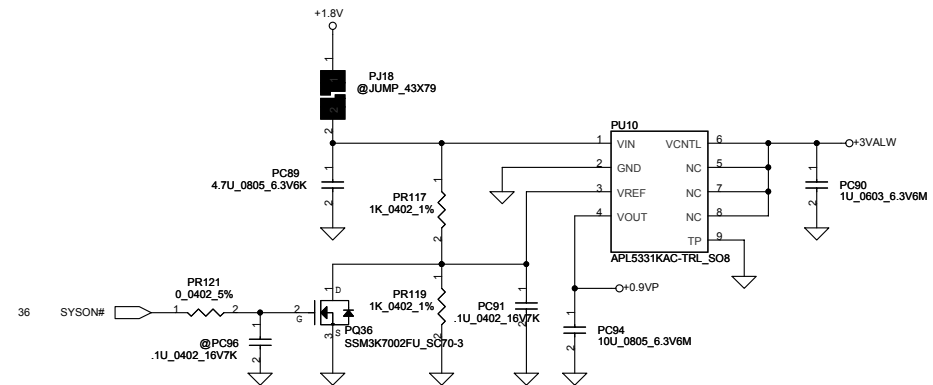
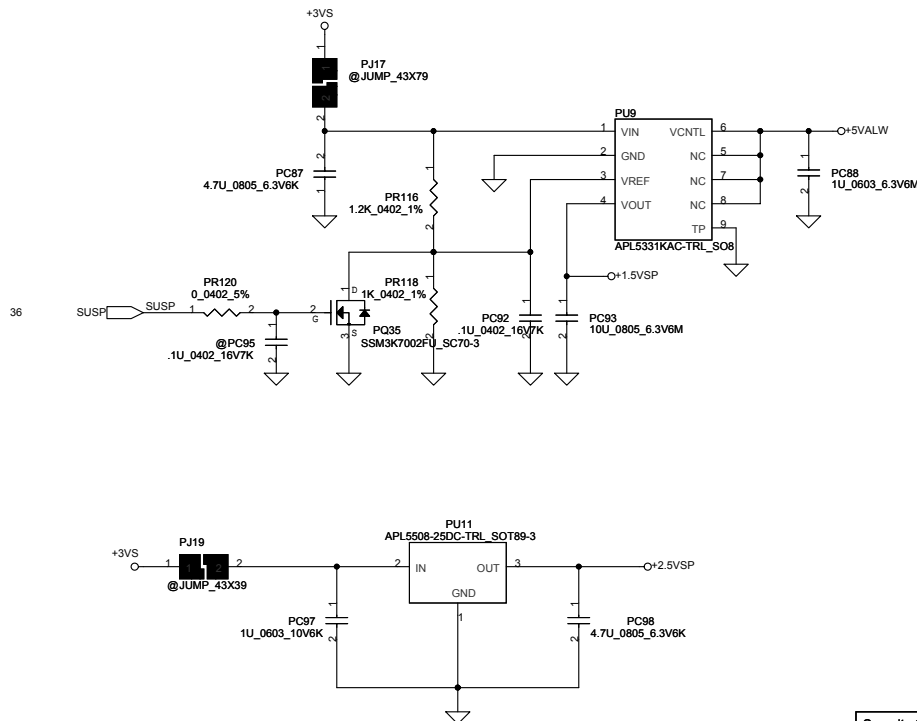


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Ipeak = 8A
Imax = 5.6A
F = 315K

Total capacitor 220uF
ESR = 15mohm



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Version Change List (P. I. R. List)for Circuit

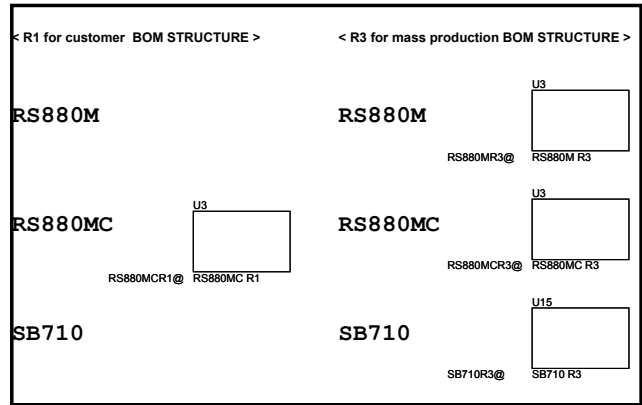
Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1.	2009/02/26	--> Change D36 from ROHM to PANJI				55. 2009/11/24 --> Modify R195, R195 BOM structure for RS880M UMA with non-HDMI function	
2.	2009/02/26	--> Remove H38, H39					
3.	2009/02/27	--> Change the footprint of T9, T10, T11, T12, T19, T20 from TPC12 to TPC24					
4.	2009/02/27	--> Change 5V power of LCD connector					
5.	2009/03/02	--> Unmount D17, R965 and mount R966					
6.	2009/03/02	--> Unmount R556					
7.	2009/03/05	--> Change side-port memory to Hynix SA00002UH00					
8.	2009/03/05	--> Change RA16 from 5% to 1%					
9.	2009/03/10	--> Change R146 from 100k ohm to 10k ohm					
10.	2009/03/10	--> Change Y2 from SJ114P3M730 to SJ114P3MG00					
11.	2009/03/11	--> Change C686, C699, C702, C705, C706, C708, CA27 from SE074221K00SE to SE074221K80 for Green part					
12.	2009/03/11	-->Change LAN_WAKE# & EC_SWI#					
13.	2009/03/12	--> Unmount USB sleep & charge, add R112 & R113					
14.	2009/03/12	--> Unmount HDMI CEC controller and related components.					
15.	2009/03/12	--> Connect USB_OC#0 to LAN_WAKE# through 0 ohm					
16.	2009/03/12	--> Change H42 from NPH to PH					
17.	2009/03/24	--> Change F2 footprint to F_MINISMDC110F-2					
18.	2009/03/24	--> Add R370 & R381					
19.	2009/03/24	--> Change R557's BOM structure from H@ to @					
20.	2009/03/24	--> Change R440 from 0 ohm to 100k ohm					
21.	2009/04/06	--> Remove PCMCIA page and function					
22.	2009/04/06	--> Add RM8 100K ohm					
23.	2009/04/06	--> Change R440 from 100K ohm to 0 ohm for Askey BT module					
24.	2009/04/06	--> Change C480's BOM structure from BT@ to @					
25.	2009/04/10	--> Add C876 for power noise issue					
26.	2009/04/10	--> Add D20 for power noise issue					
27.	2009/04/10	--> Replace PJ13, PJ30, PJ14, PJ15, PJ16 by PL17, PL18, PL19, PL20, PL21					
28.	2009/04/20	--> Change D12's BOM structure to @					
29.	2009/04/22	--> Change C876 & C234 PN from 330u to 470u (SGA00001U00) for Power noise issue					
30.	2009/04/28	--> Add PCMCIA function on page 27					
31.	2009/04/29	--> Change R42's BOM structure to @					
32.	2009/05/06	--> Change C876 & C234 from 470u to 330u for COST reduce					
33.	2009/05/07	--> Mount R367 for can't power on issue (AMD SB leakage)					
34.	2009/05/18	--> Change RA38's BOM structure from LVDSSET@ to @					
35.	2009/05/19	--> Change C876 from SGA00001Q80 to SGA19331D00					
36.	2009/05/19	--> Add C618 & C619 for EMI request					
37.	2009/06/03	--> Change PJP9 to L90 (SM010024220) for EMI request					
38.	2009/06/03	--> Add C120 for EMI request					
39.	2009/06/03	--> Add C618, C619 for EMI reserve					
40.	2009/06/03	--> Combine camera with LVDS Delete R430, R428, R20, R18, C744, JCAM					
41.	2009/06/03	--> Change BOM structure of RA31 and CA34 from @ to mount for EMI require					
42.	2009/06/03	--> Add CA58 for EMI reserve					
43.	2009/06/03	--> Delete JPWR1 for ME portion					
44.	2009/06/04	--> Change UL3 from SP050005V00 to SP050005W00 (for AP issue)					
45.	2009/06/10	--> Change R125 and R625 BOM Structure from @ to NSIDE@					
46.	2009/07/07	--> Change C643 and C652 value from 18P to 12P					
47.	2009/07/07	--> Change C350 from SF22001M200 to SF000001H00 as main source					
48.	2009/08/06	--> Change Y7 from SJ100003D00 to SJ132P7KW10 for green review					
49.	2009/08/11	--> Change RN3 BOM Structure from EXPCARD@ to always mount on and relocated to SB side (Page 20).					
50.	2009/09/21	--> Change CL26, CL27 from SE00000H180 to SE074102K80, due to shortage					
51.	2009/09/21	--> Change C9, C13, C70, C71, C83, C84, C95, C104, C120 from SE068102J80 to SE074102K80, due to main source shortage					
52.	2009/09/21	--> Change U34, U36 from SA00001WP00 to SA00003GI00, due to main source E3 code					
53.	2009/10/02	--> Delete RN2's BOM structure and move to SB side (Page 21).					
54.	2009/10/12	--> Change Q13,Q17 PN to SB770020010 for common use					

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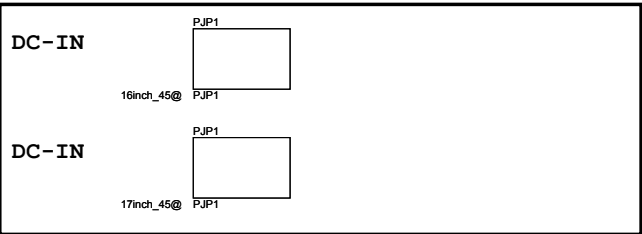
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HW4 Product Improvement Record (P.I.R.)

< Tigris >



< DC Jack >



< PCB >

